Switched Doherty PAs for 3G

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Outline

- Introduction and motivation
- Pros and Cons
- Background: Stepped bias and switched periphery
- Switched Doherty
- Example PAs
- Performance improvement techniques
- Test data
- Tristate switched Doherty PA in BiHEMT process
- Conclusion

Why Use Switched Doherty PAs?

- CDMA talk-time is strongly influenced by PA current
- Average PA current is dependent on power efficiency at low power levels (in addition to full power PAE)
- Improvement in low power PAE requires:
  - a reduction in supply voltage *OR*
  - an increase in load impedance (compared to full power levels)
- Load impedance can be changed explicitly (switched) or implicitly (periphery switching)
- The results reported here use implicit load control to improve low power efficiency

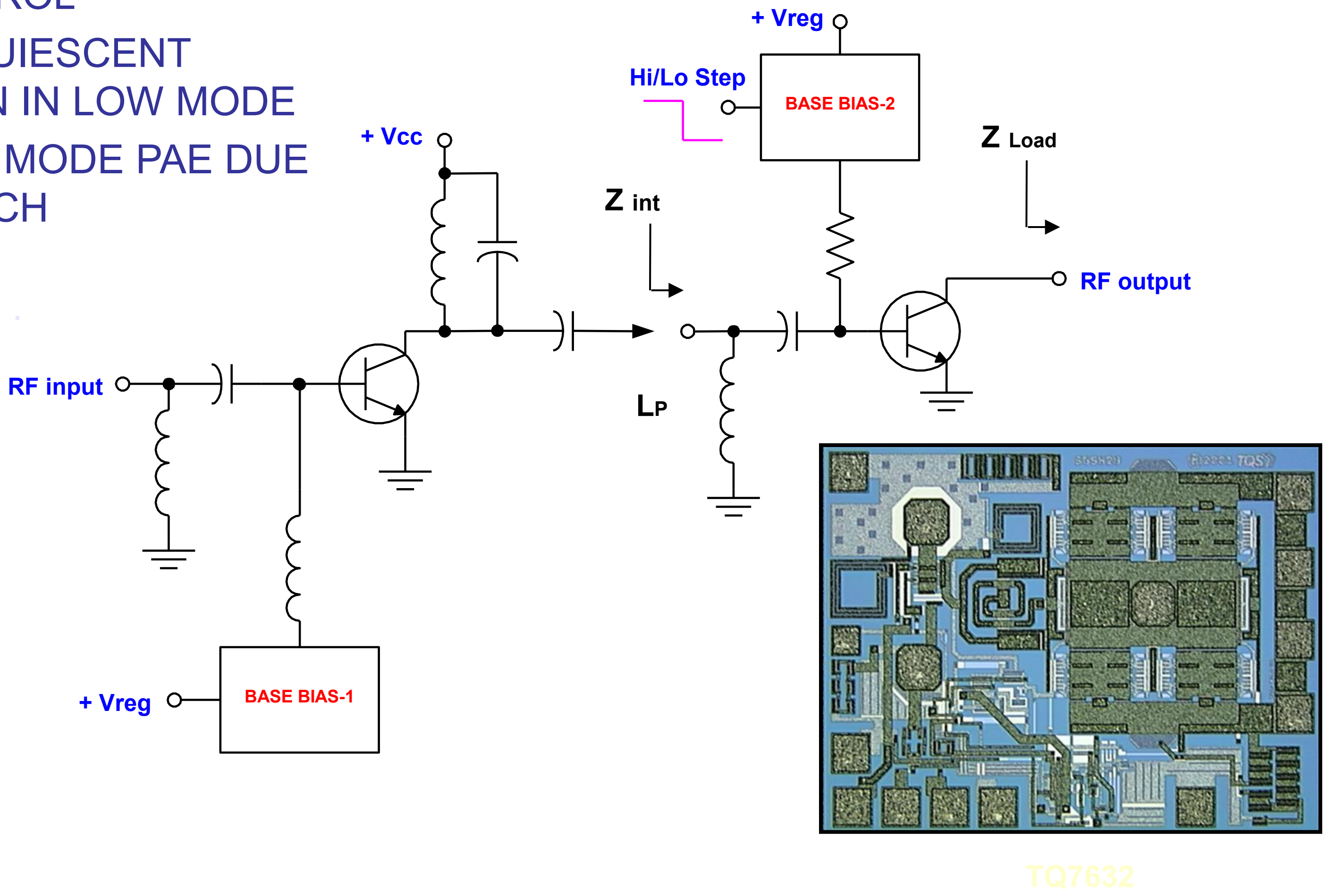
Pros and Cons

- Switched Doherty PAs are not easy to implement
  - Z inverter (Zo and insertion phase)
  - Delay line (Zo and insertion phase)
  - Interstage branch impedances
  - *ALL MUST BE CORRECT- consistent with final stage segmentation*

- Performance advantages include:
  - High PAE in <u>both</u> low and high power modes
  - No insertion phase discontinuity during mode change
  - Increased load insensitivity and superior 3rd order reverse IMD due to quadrature operation in high power mode
  - All periphery is used in high power mode
  - External load impedance is same as conventional PA

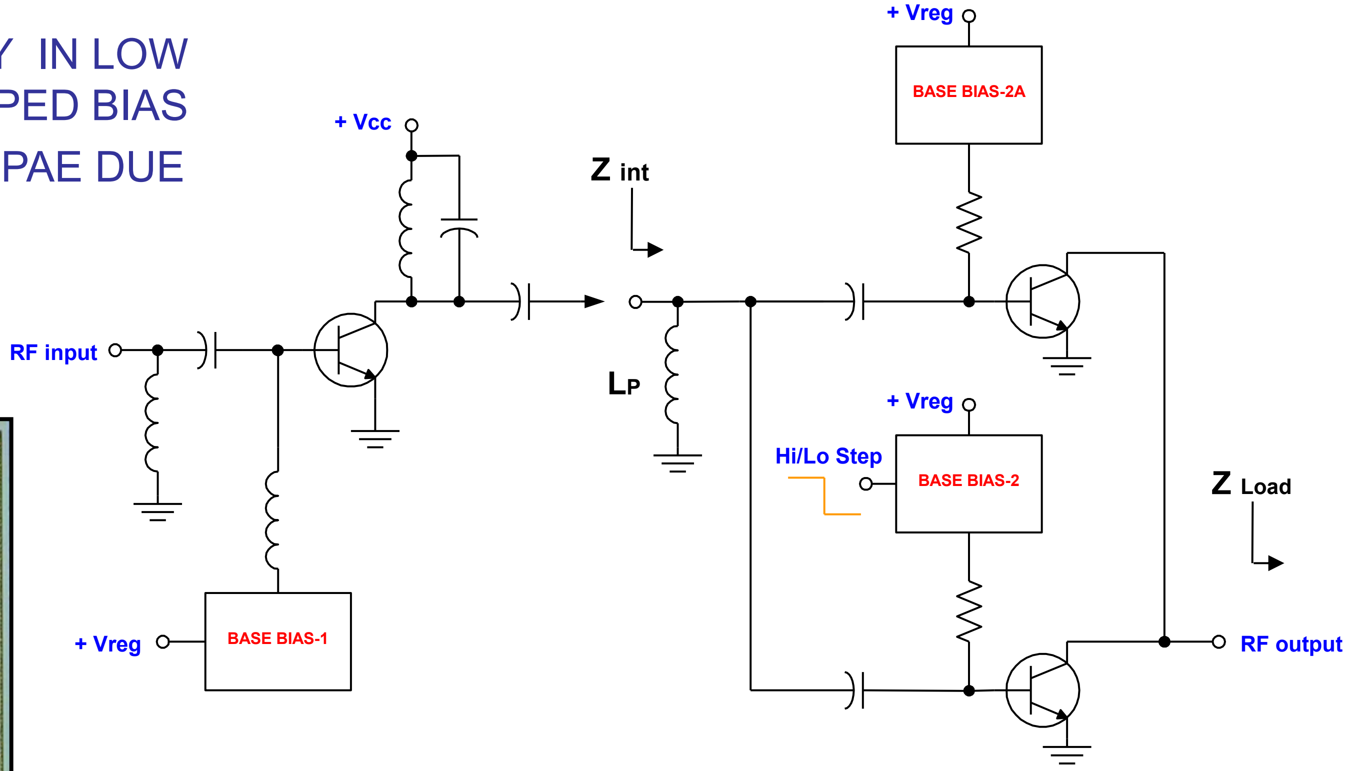
Background: Conventional PA with Stepped Bias

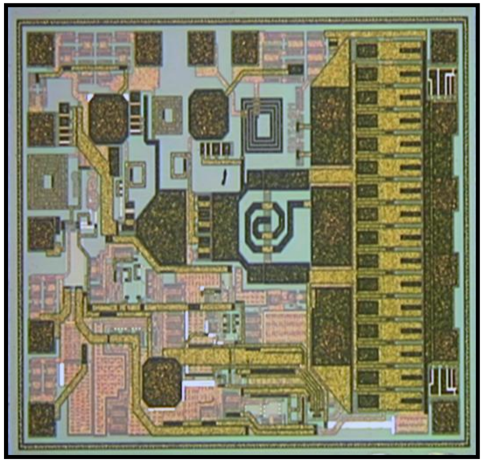
- 1st GENERATION CONVENTIONAL PA
- 1-BIT CONTROL
- ONLY DC QUIESCENT REDUCTION IN LOW MODE
- POOR LOW MODE PAE DUE TO MISMATCH



Background : Conventional PA with Switched Periphery

- 2^{nd} GENERATION CONVENTIONAL PA
- 1-BIT CONTROL
- BETTER LINEARITY IN LOW MODE THAN STEPPED BIAS
- POOR LOW MODE PAE DUE TO MISMATCH





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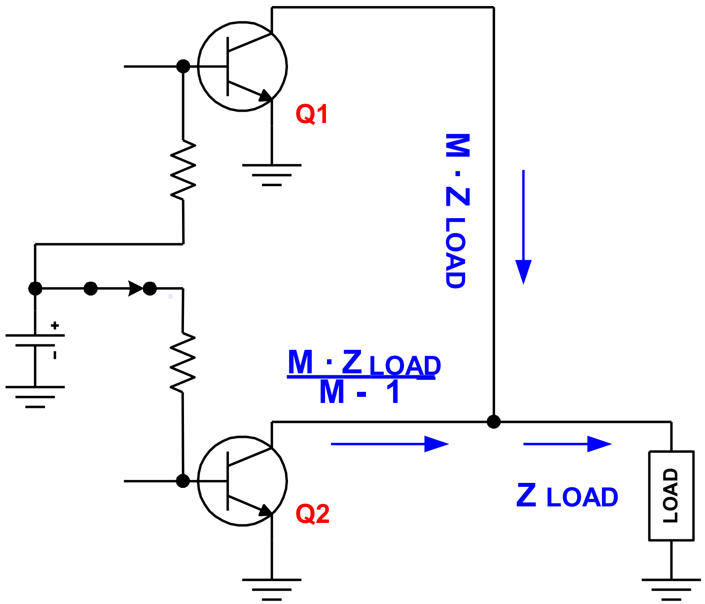
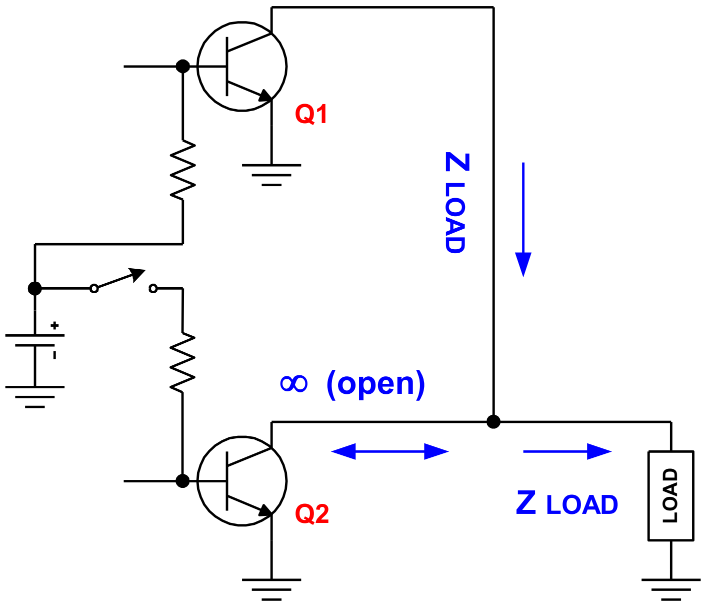
Switched Periphery Load Sharing

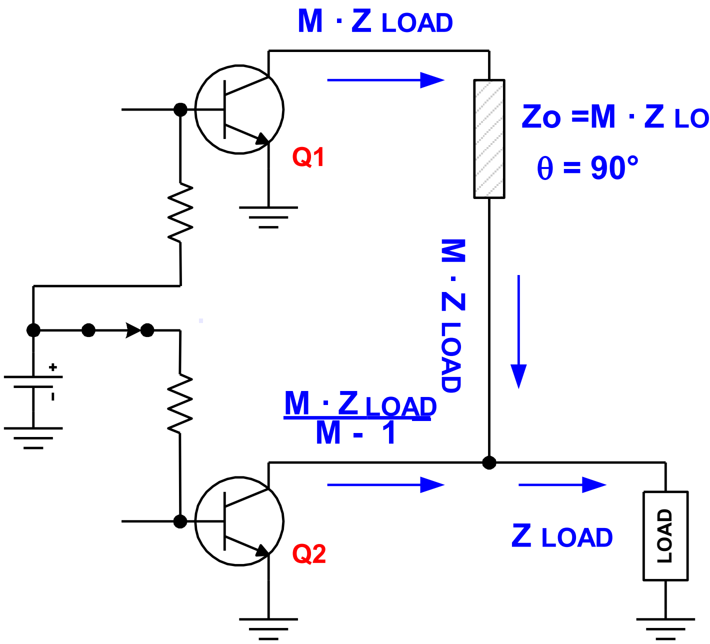


HIGH POWER MODE

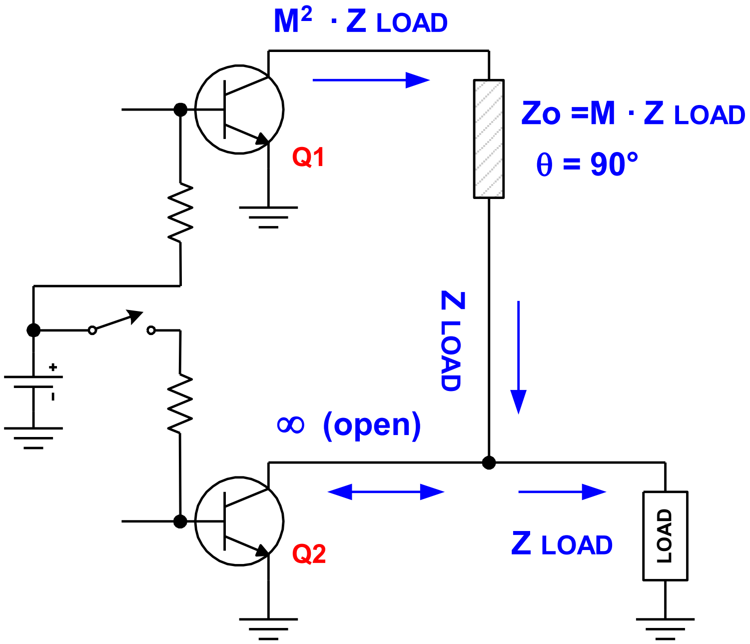


LOW POWER MODE

Switched Doherty Load Sharing

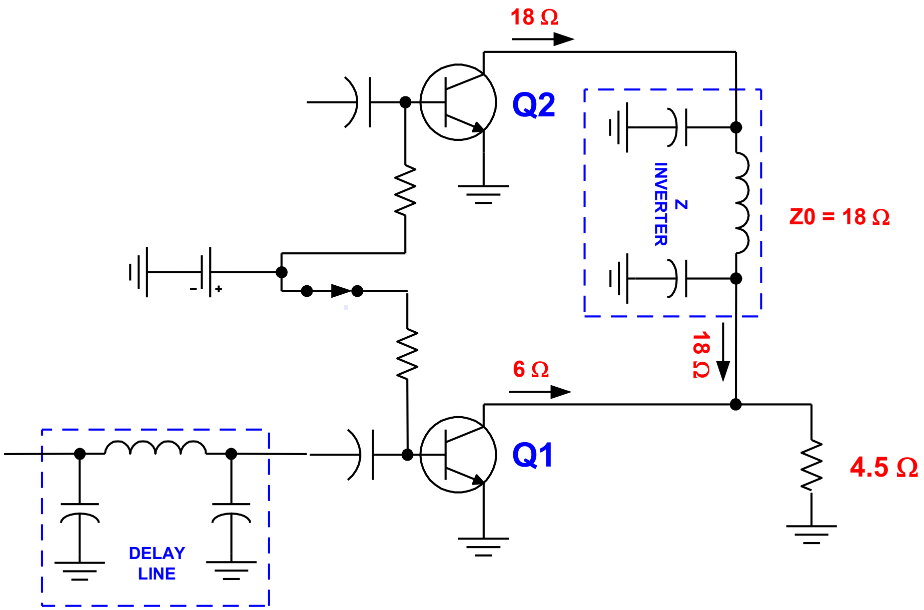


HIGH POWER MODE

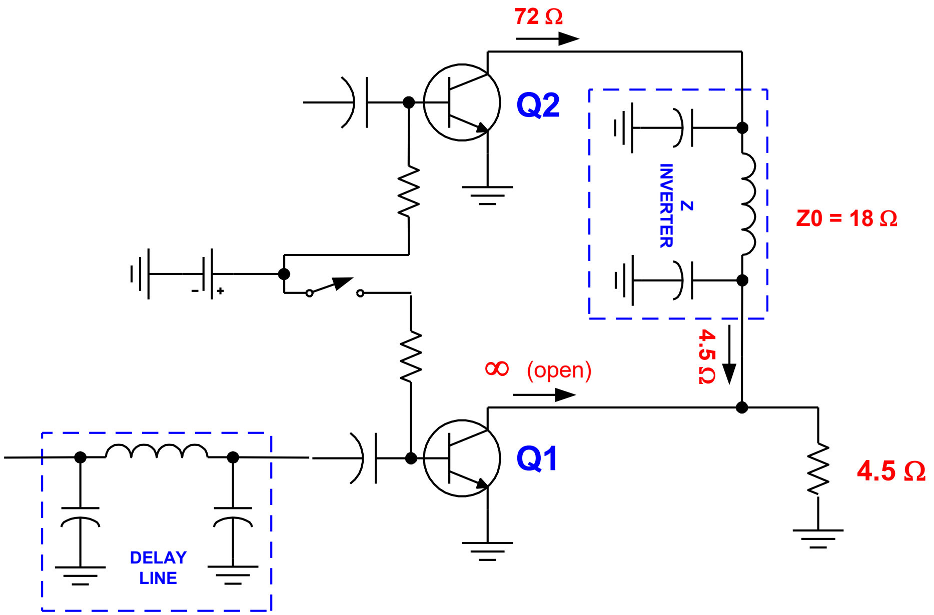


LOW POWER MODE

CDMA Load Sharing Prototype

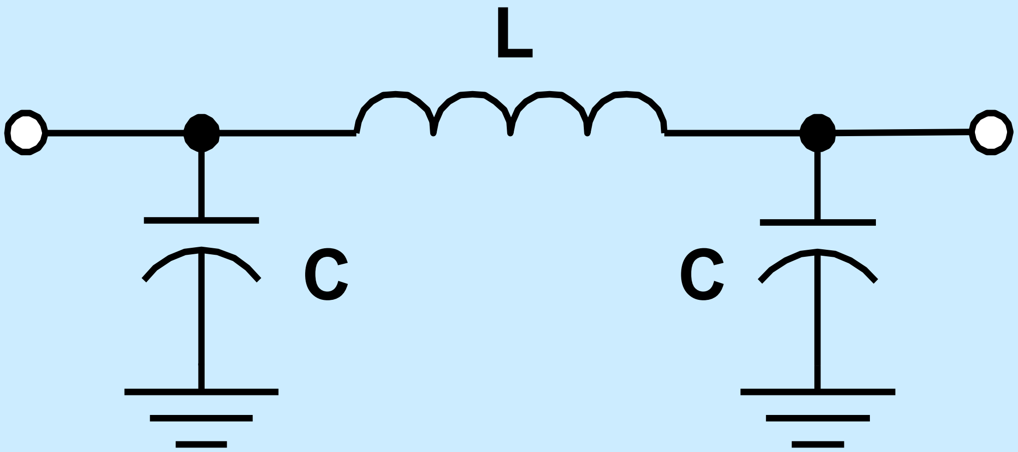


HIGH POWER MODE



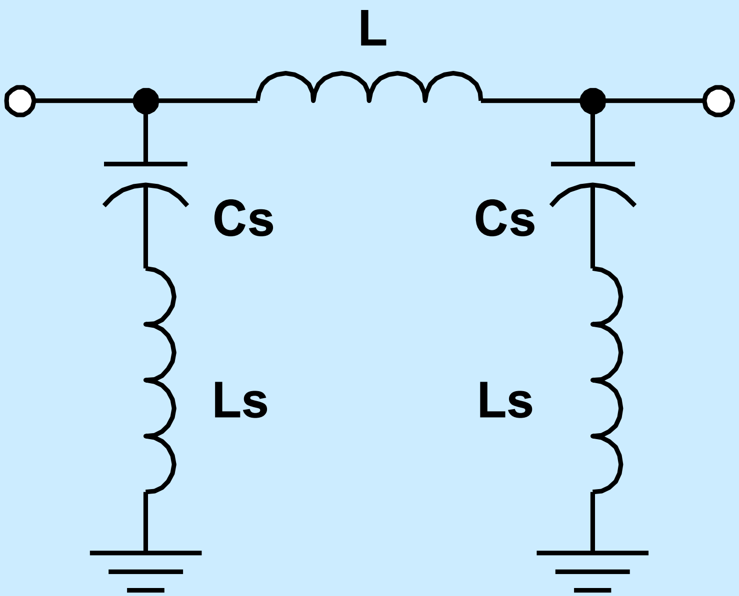
LOW POWER MODE

Constant-K LC Impedance Inverter



$$L = Z_0/\omega_0, \quad C = (\omega_0 Z_0)^{-1}$$

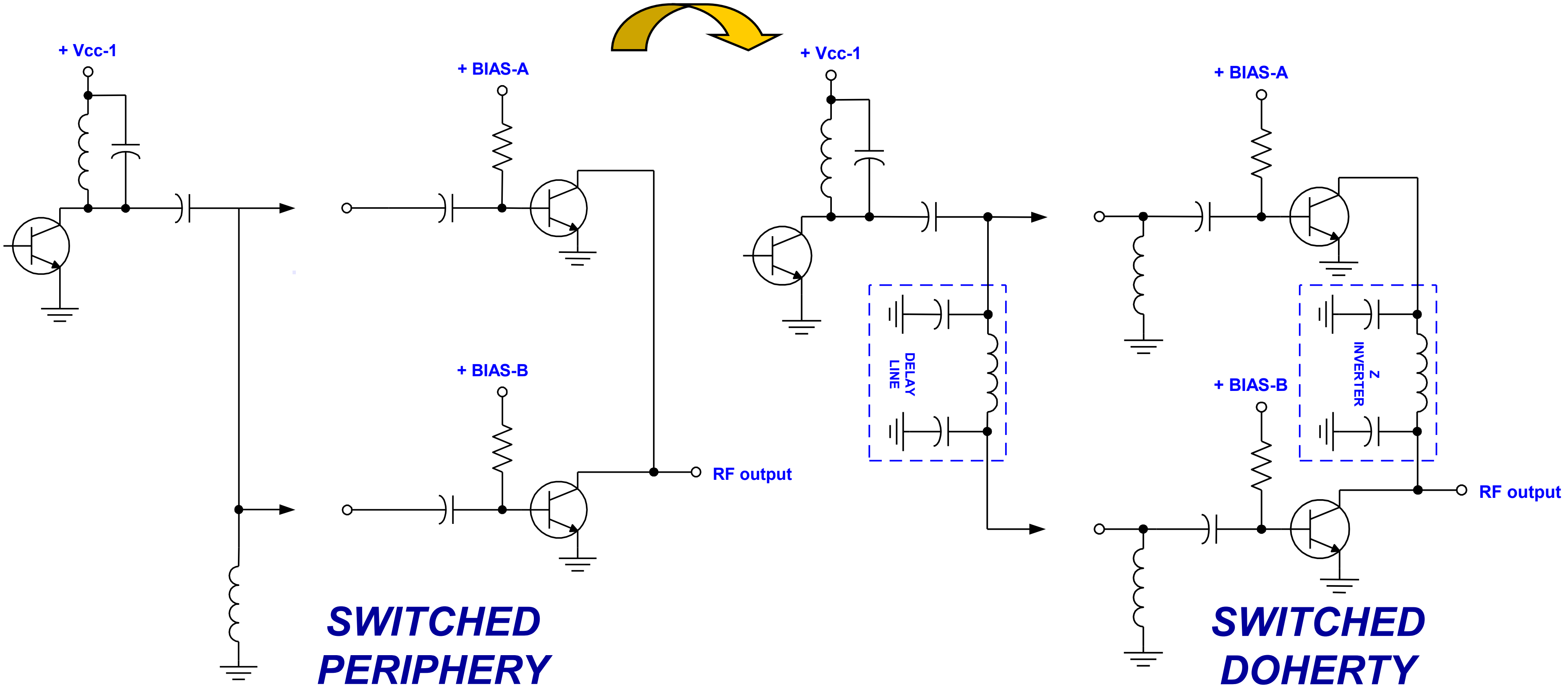
M-derived LC Impedance Inverter



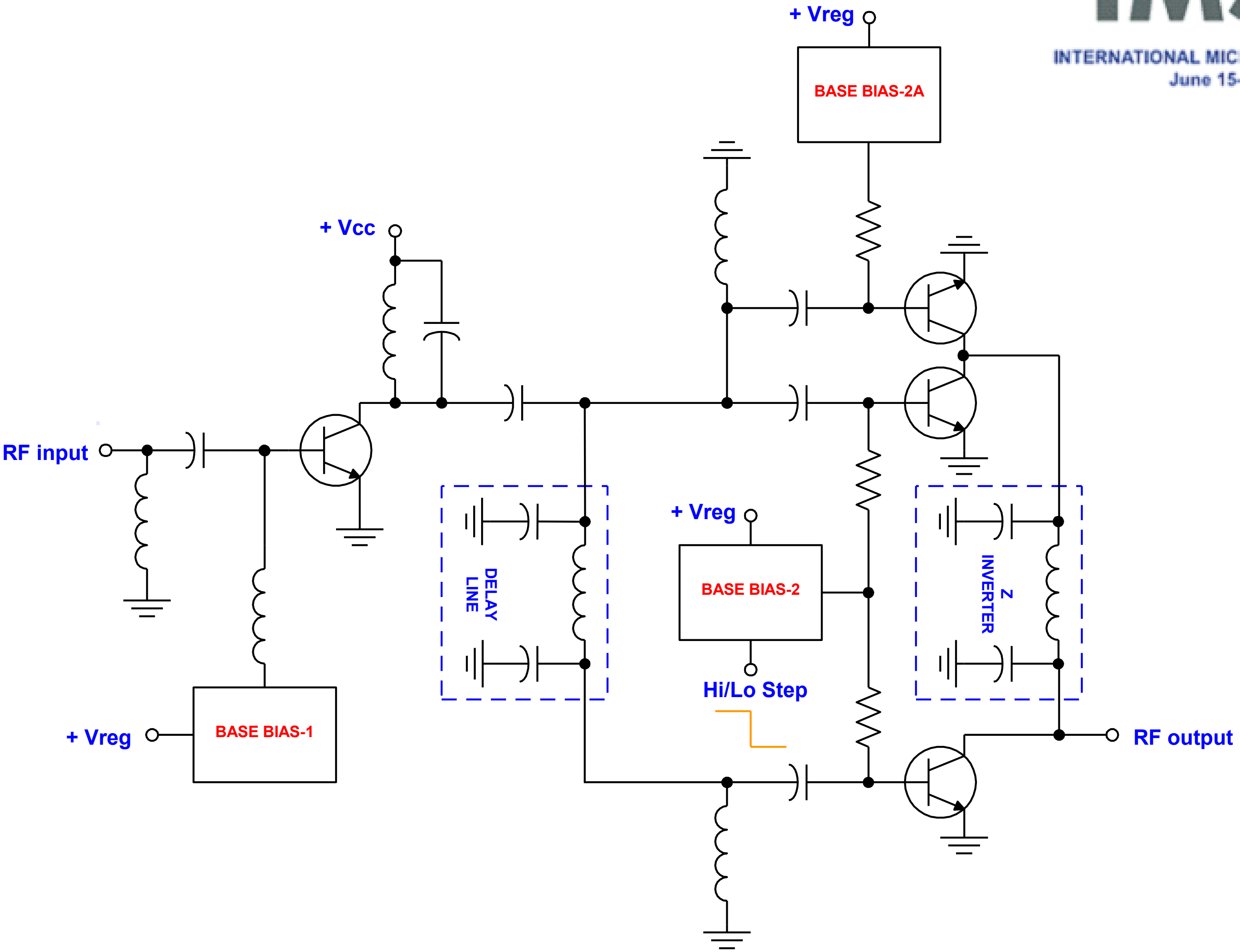
$L = Z_0/\omega_0$, $L_s = Z_0(3\omega_0)^{-1}$, $C_s = 3(4\omega_0 Z_0)^{-1}$

TRAP RESONANCE SET TO 2nd HARMONIC

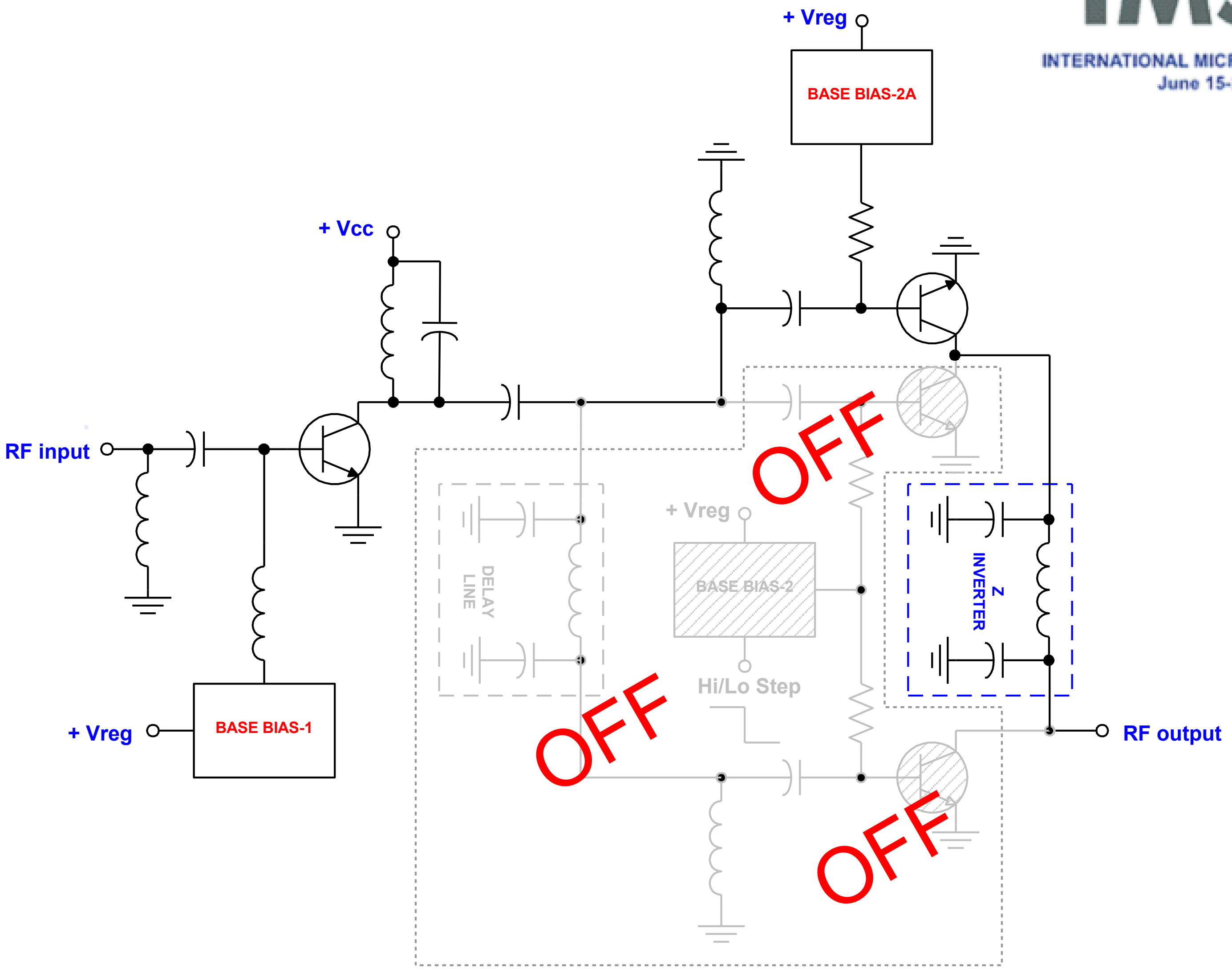
Switched Periphery *to* Switched Doherty



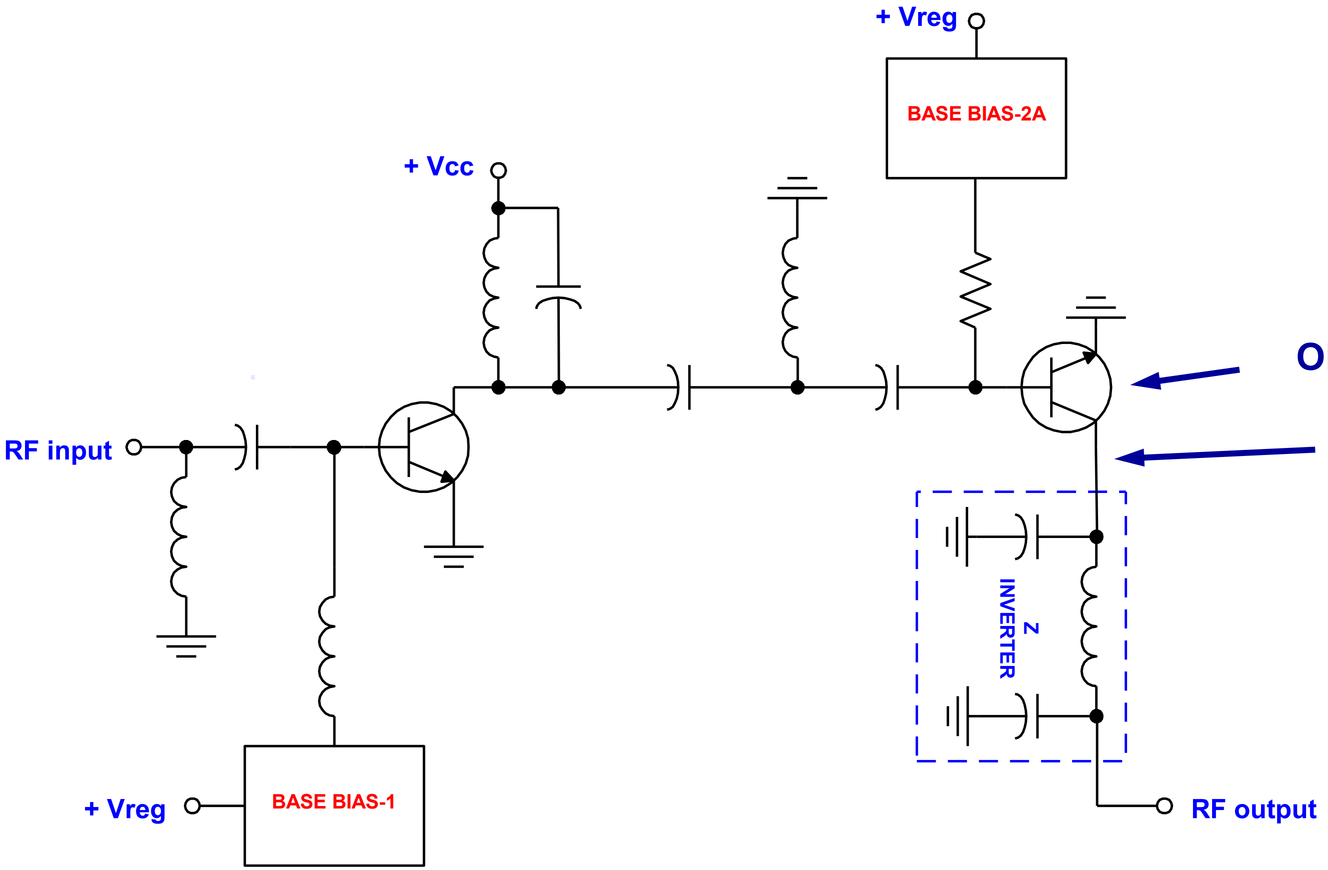
Switched Doherty PA



Low Power Mode



Low Power Mode

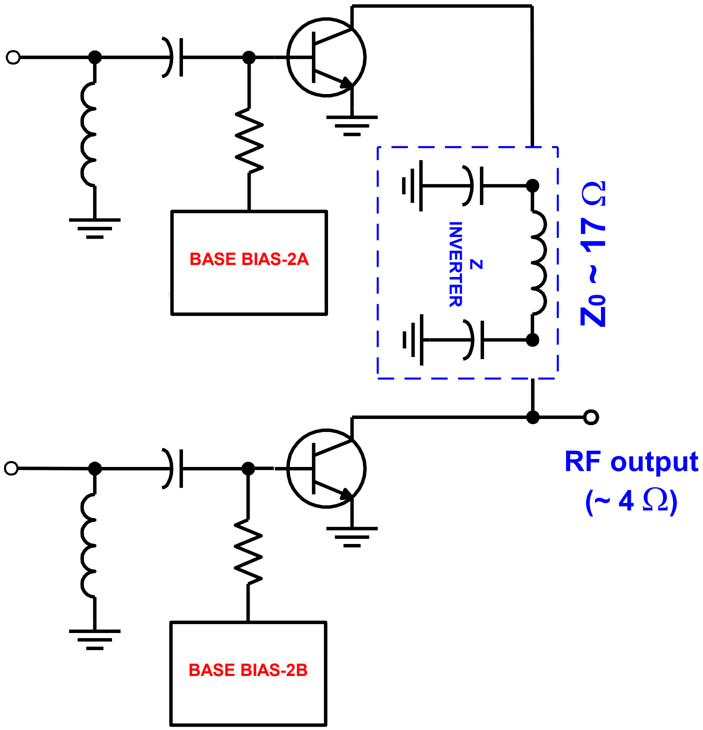


OPTIMUM PERIPHERY
AND
OPTIMUM LOAD

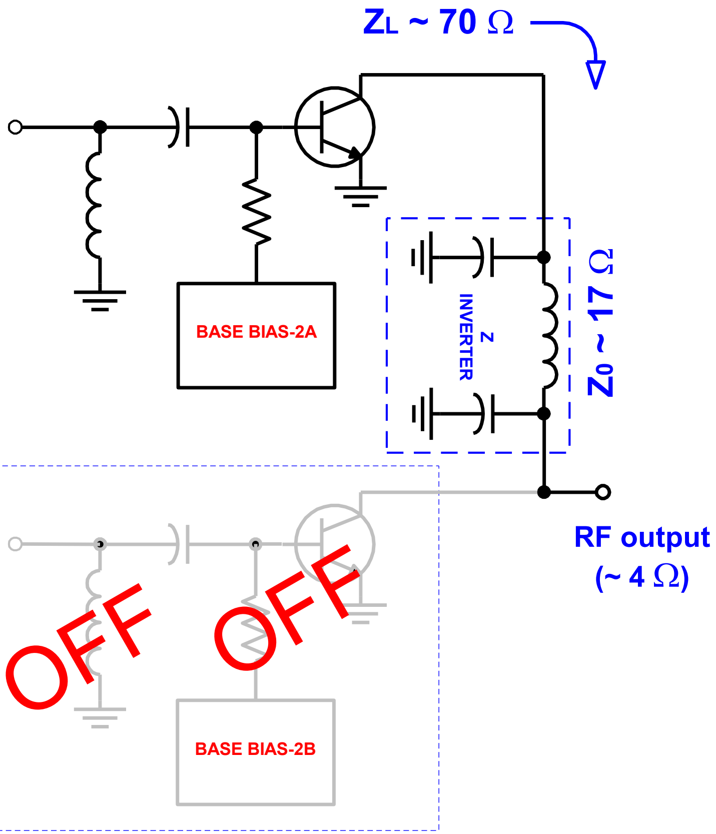
INTERNATIONAL MICROWAVE SYMPOSIUM
June 15-20, 2008

Contrast with Other Techniques

SWITCHED DOHERTY IS DUAL PATH SPECIAL CASE

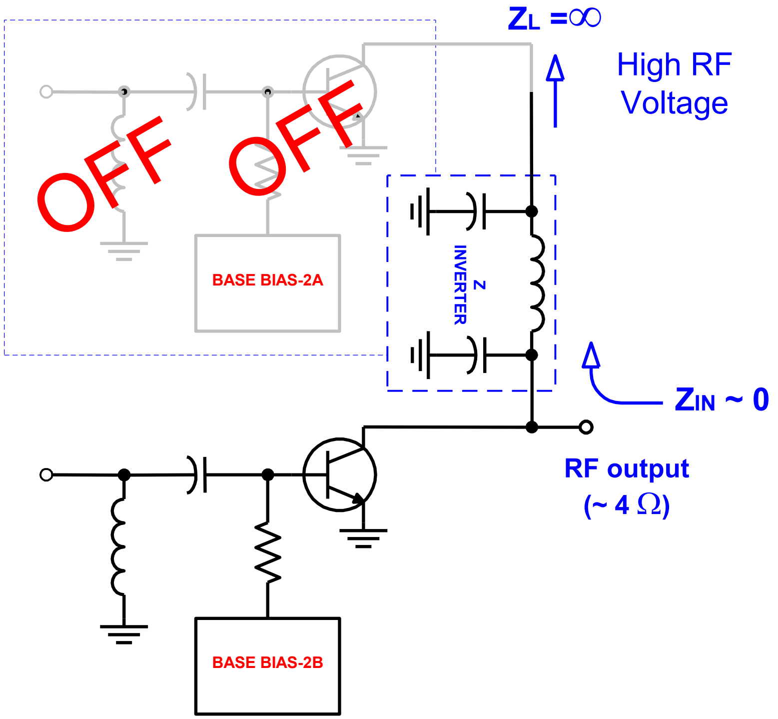


DUAL PATH ARCHITECTURE

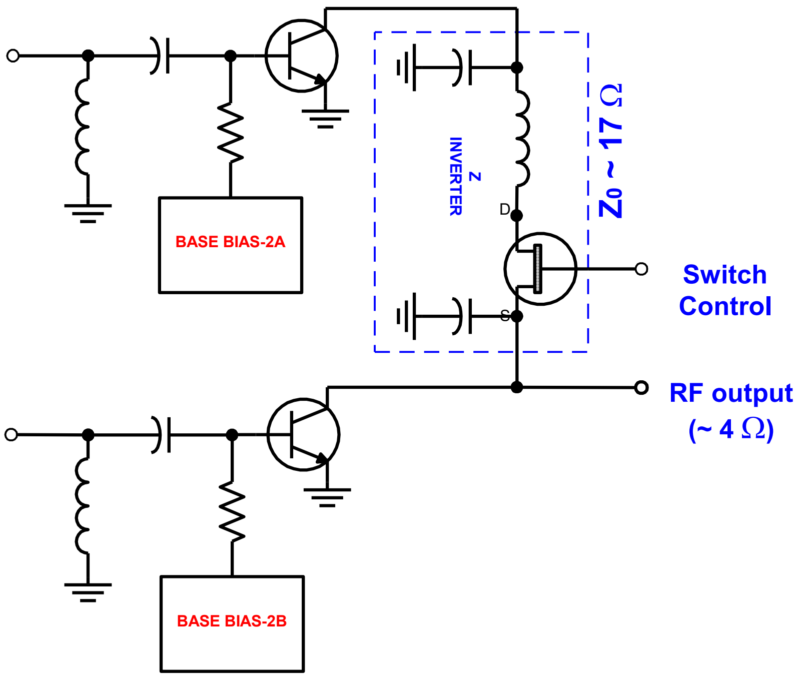


LOW POWER MODE

Contrast with Other Techniques *(continued)*

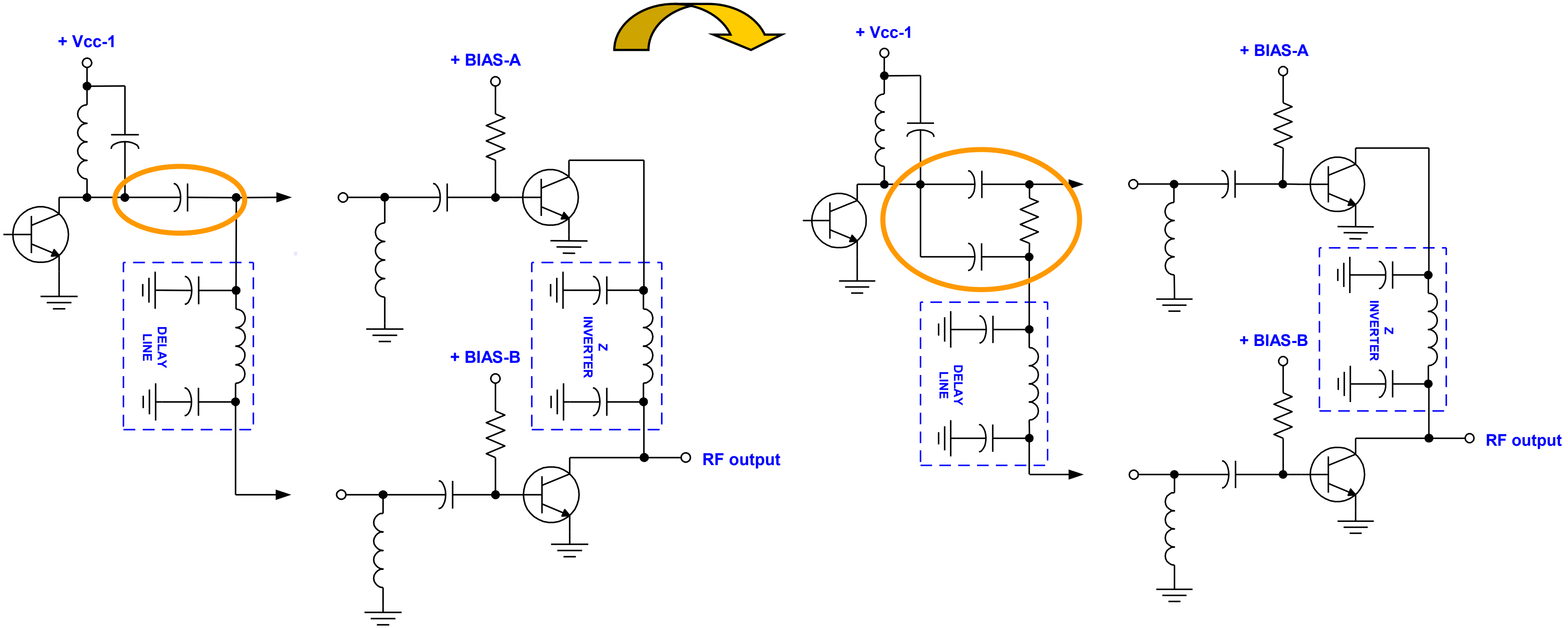


DISTORTION IN HIGH POWER MODE



SWITCHED DUAL PATH

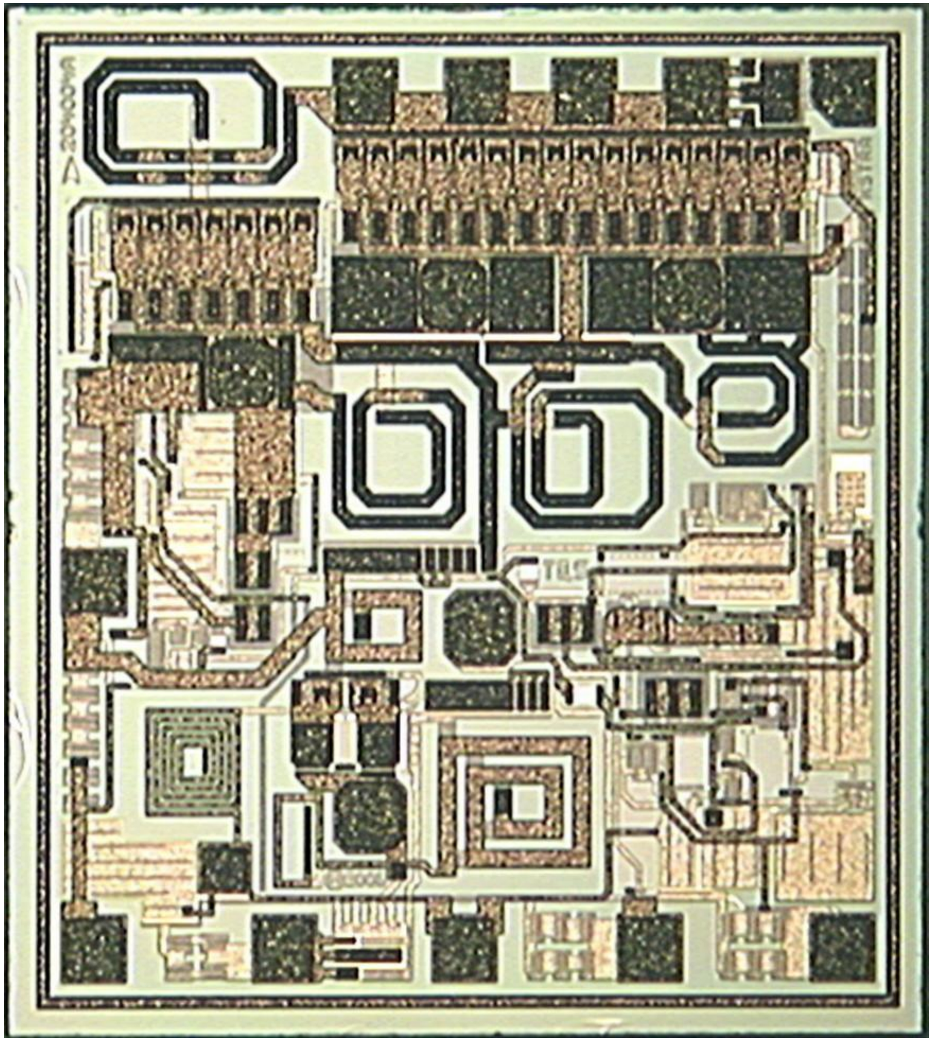
Isolation at Interstage Split



NO ISOLATION

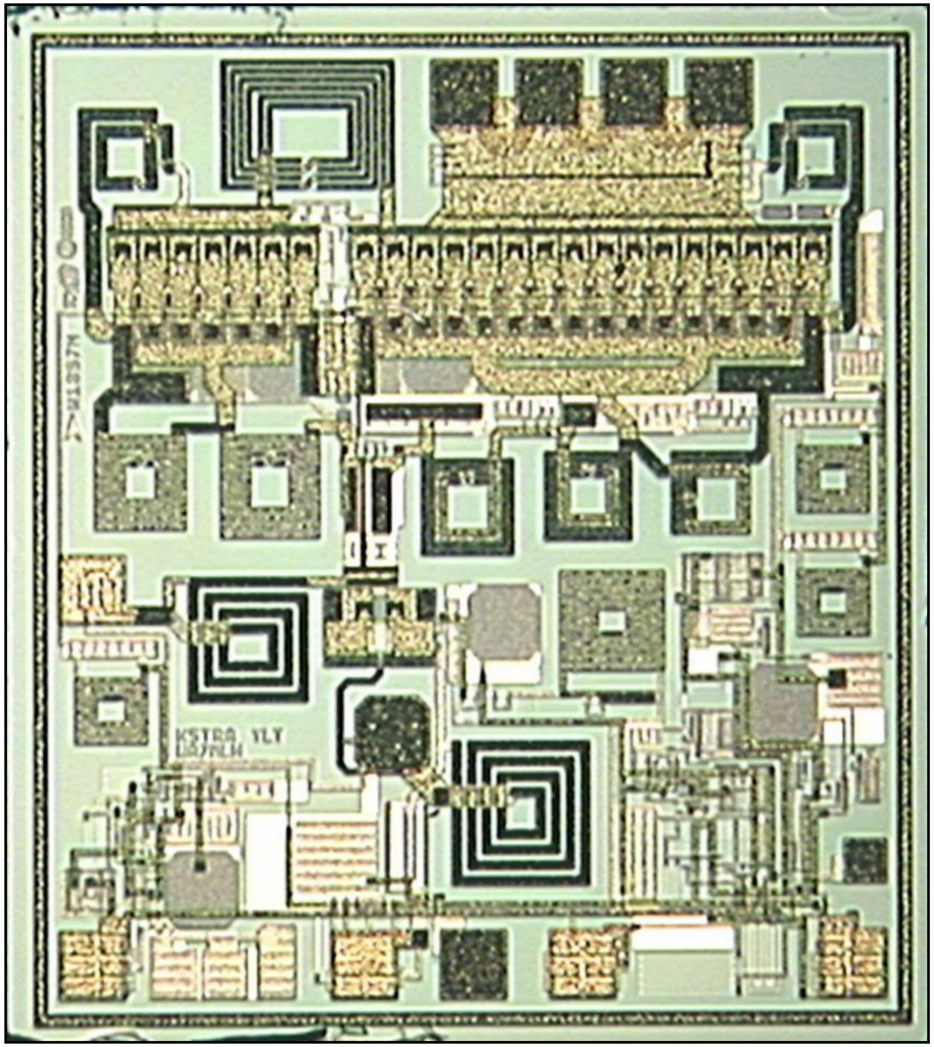
WITH ISOLATION

PCS 1ST Generation Switched Doherty



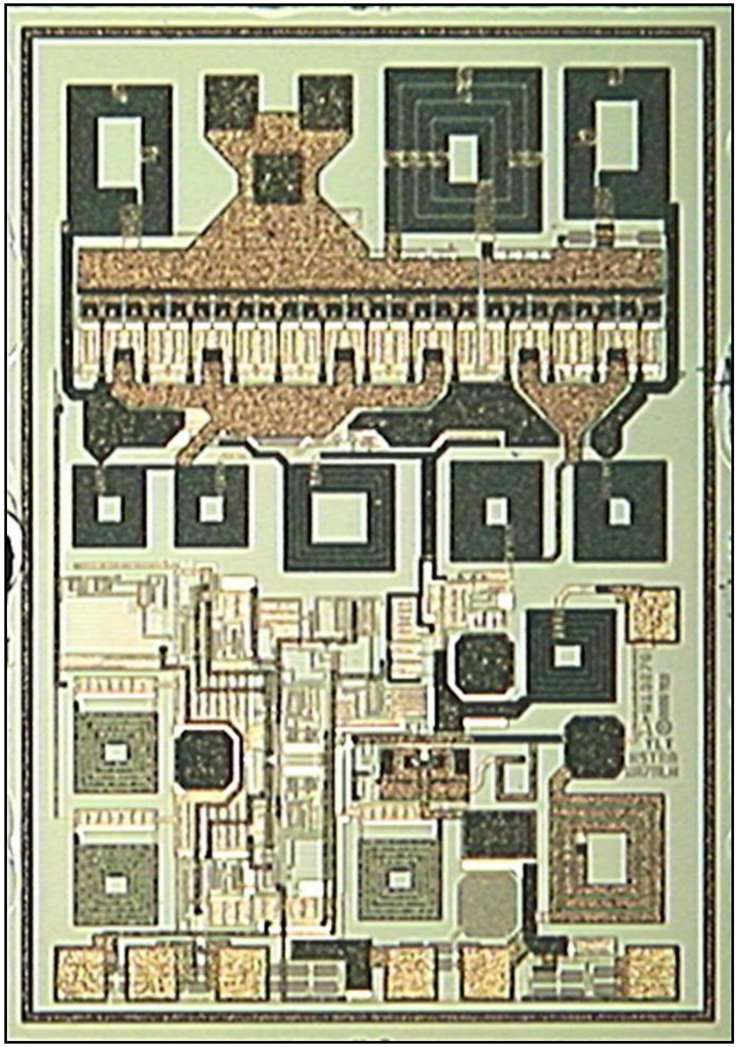
- 1120 x 1200 um^2
- 6480 um^2 final
- 550 um^2 driver
- external 2nd harmonic tuning

PCS 2ND Generation Switched Doherty



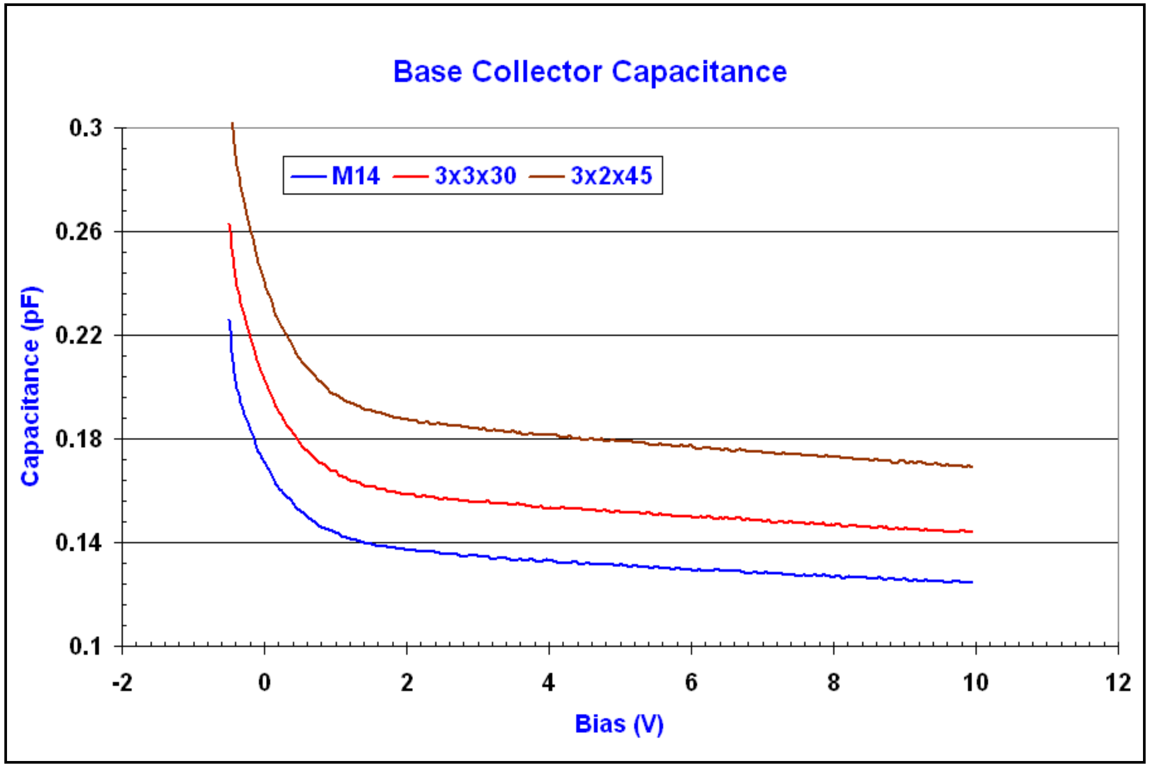
- 1170 x 1230 um^2
- 6480 um^2 final
- 550 um^2 driver
- internal 2nd harmonic tuning

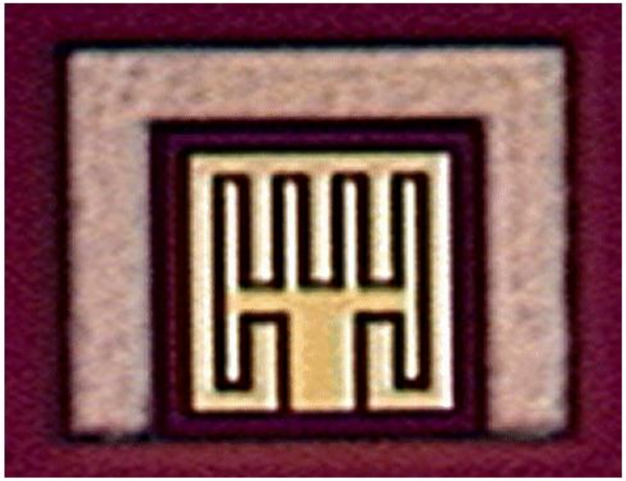
Cellular 2ND Generation Switched Doherty



- 1120 x 1470 um^2
- 6480 um^2 final
- 550 um^2 driver
- internal 2nd harmonic tuning

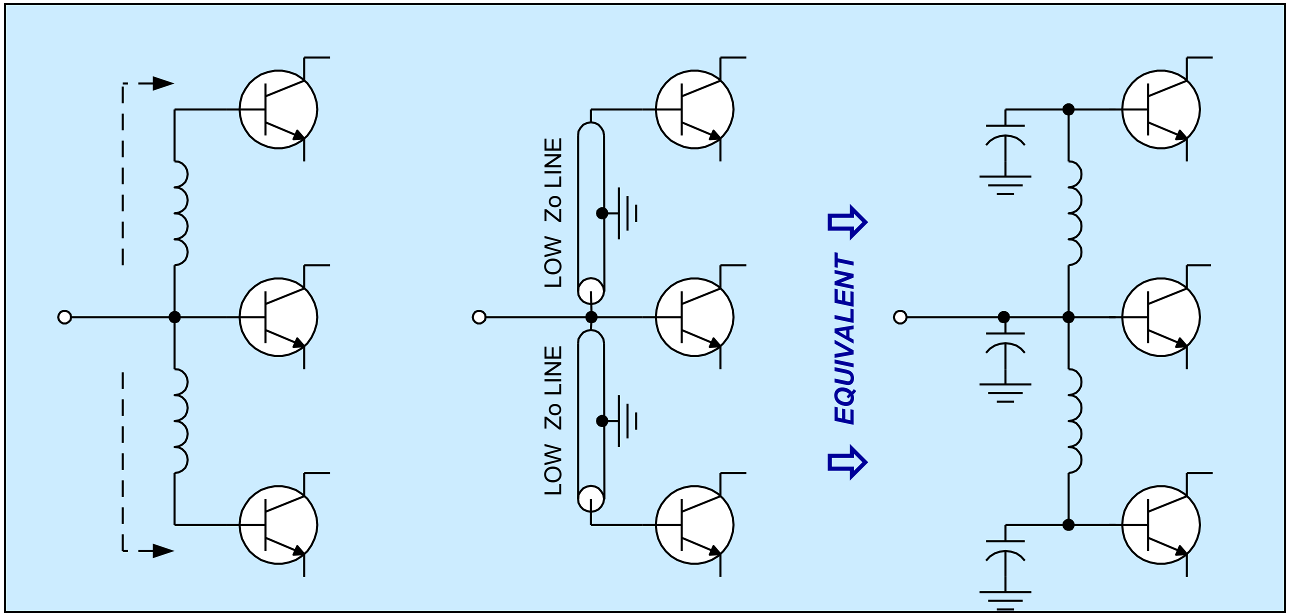
FISHBONE BASE Geometry for Low C_{BC}





- 75% of *STANDARD CELL* C_{BC}
- 57% of *HAIRPIN CELL* Rb’
- SOA is 2X *HAIRPIN CELL*
- >1 dB gain increase
- >2 % η_a increase

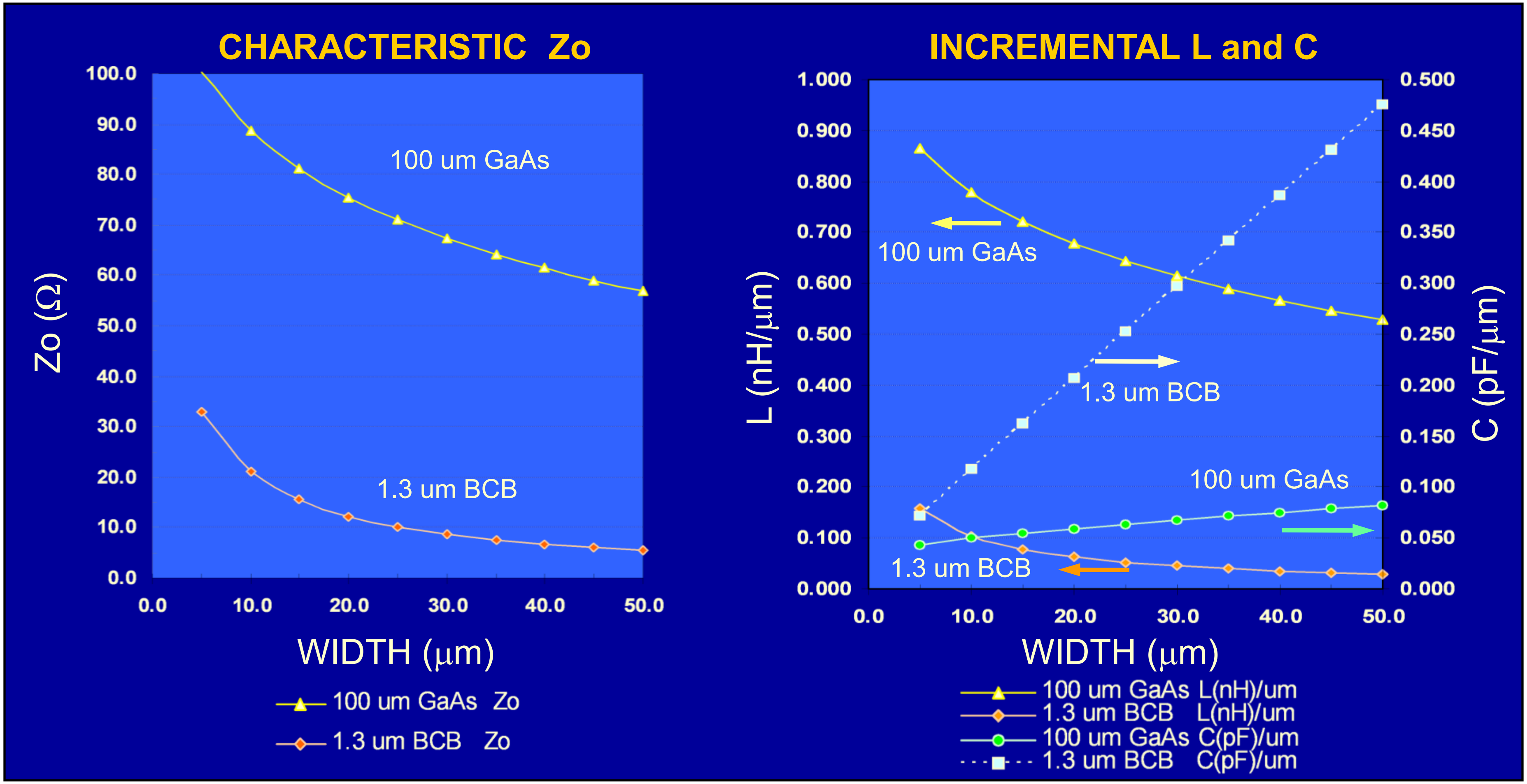
Low Inductance Base Manifold



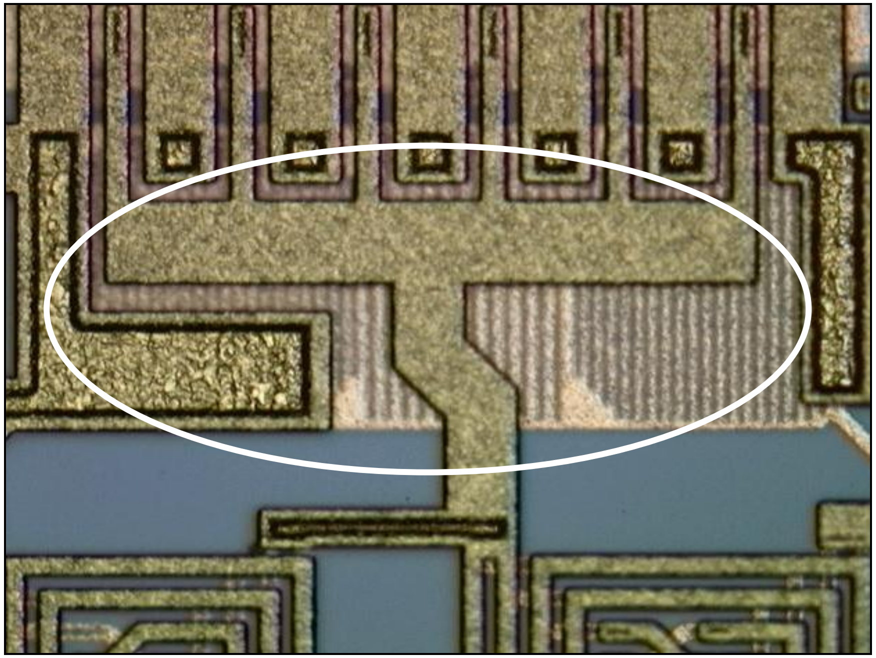
Large base $L_B \pm \Delta L_B$ ***Low $L_B \pm \Delta L_B$***   ***Low $L_B \pm \Delta L_B$***

- Lateral manifold contributes to L_B
- A low Zo transmission line can reduce L_B
- This is realized with ***METAL-2 / BCB / METAL-1*** stack
- Increased shunt capacitance is parasitic result
- Lumped equivalent model is convenient

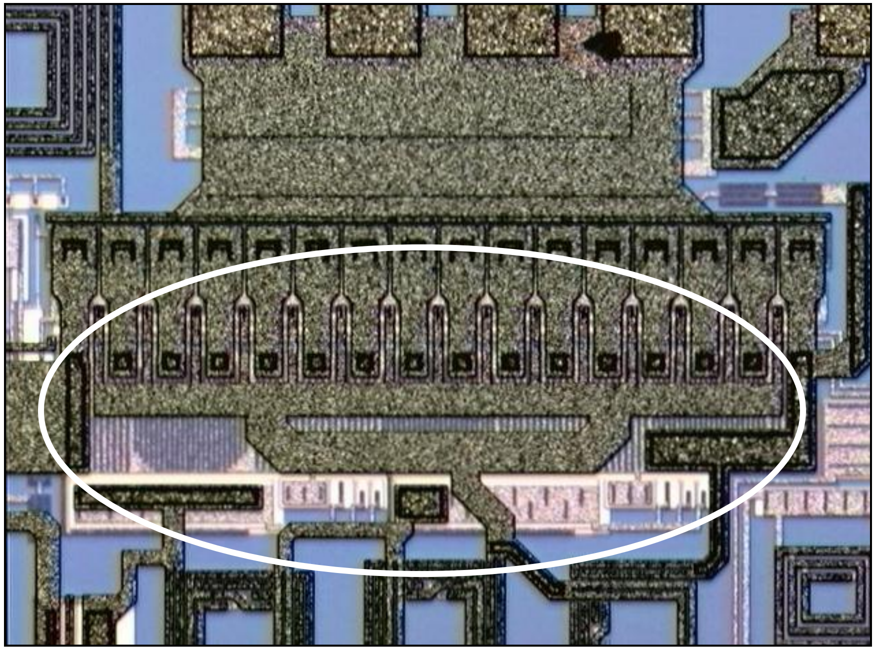
Low Interconnect L from Low Zo Lines



Low Zo Base Manifold - PCS Band

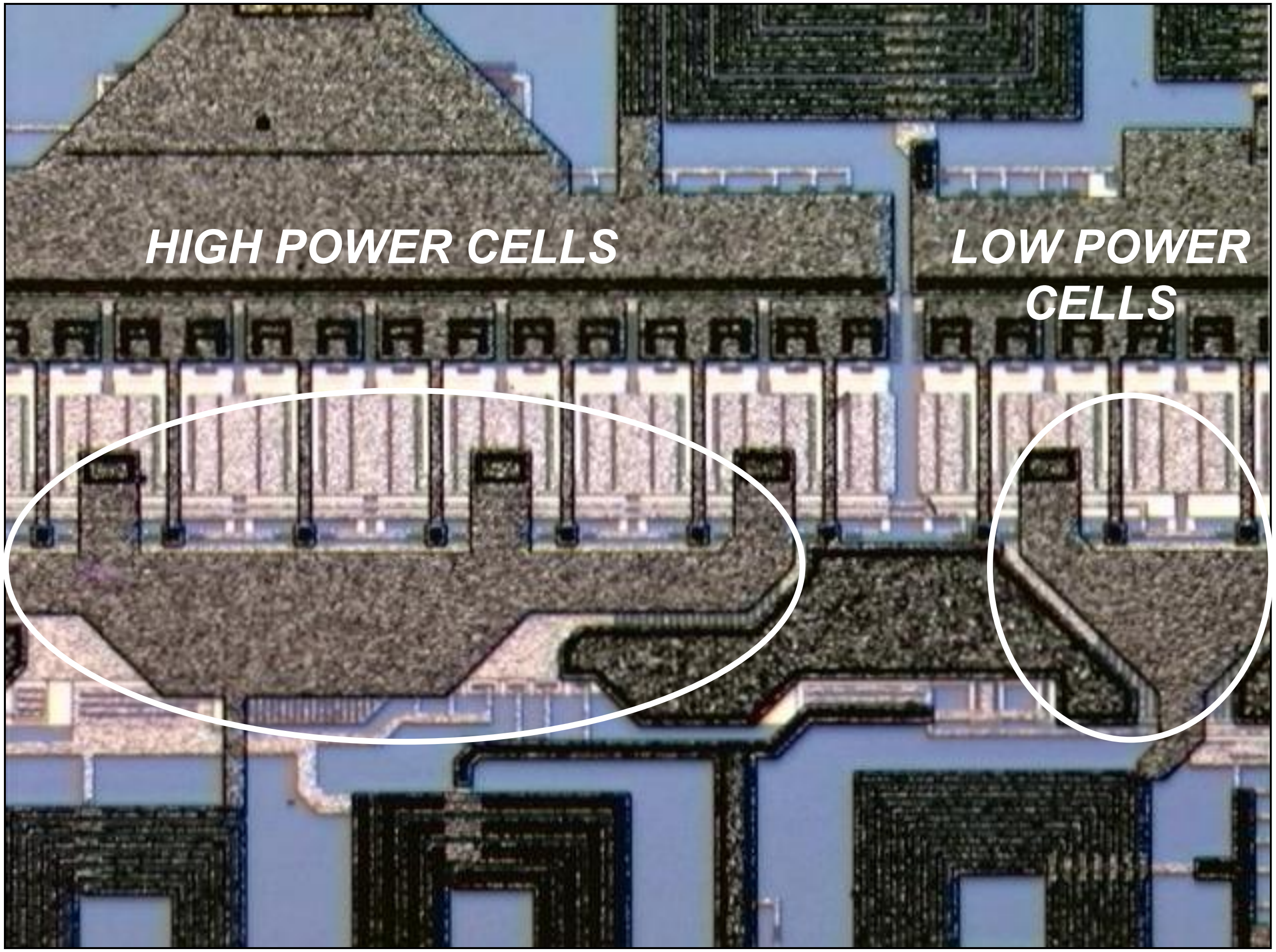


LOW POWER CELLS



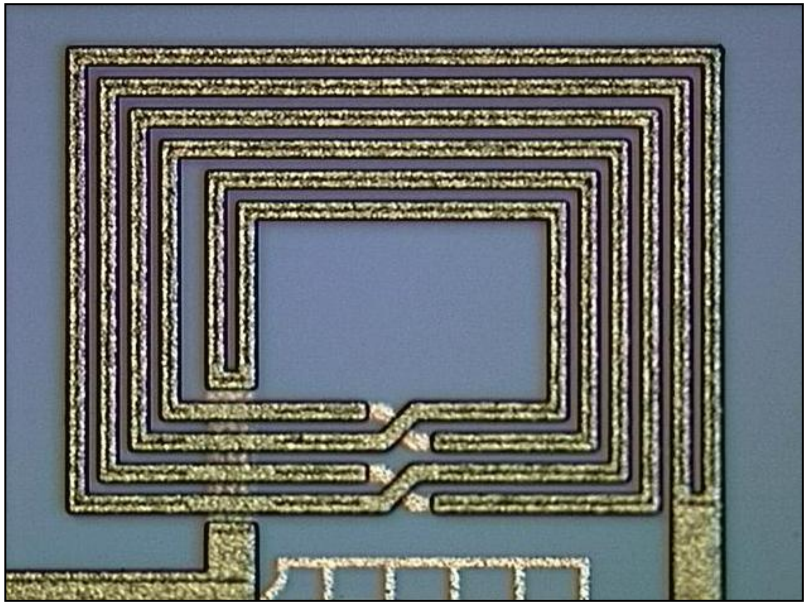
HIGH POWER CELLS

Low Zo Base Manifold - Cellular Band

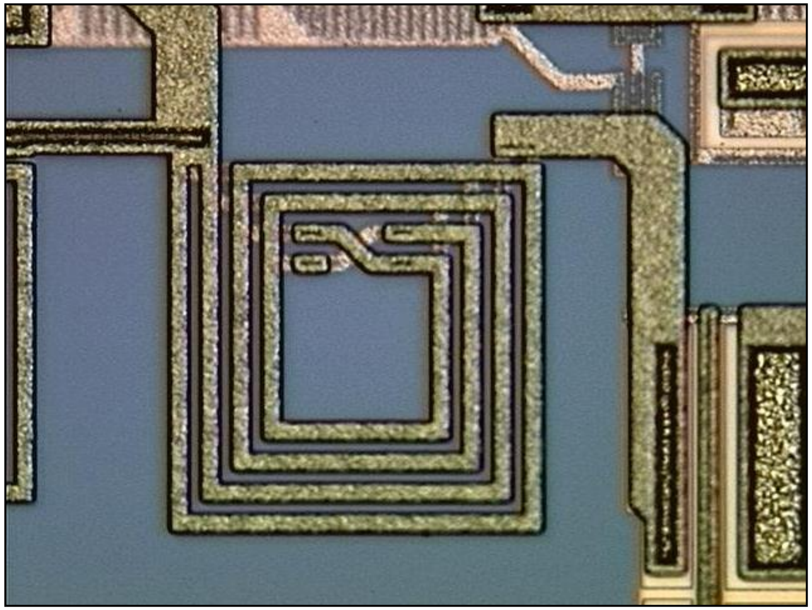


Improved Inductors

- Standard overlay increases L but looses Q
- Split and split-overlay increase Q
- Split singles loose area efficiency
- Split-overlay and hybrids are the best overall for good Q with area efficiency

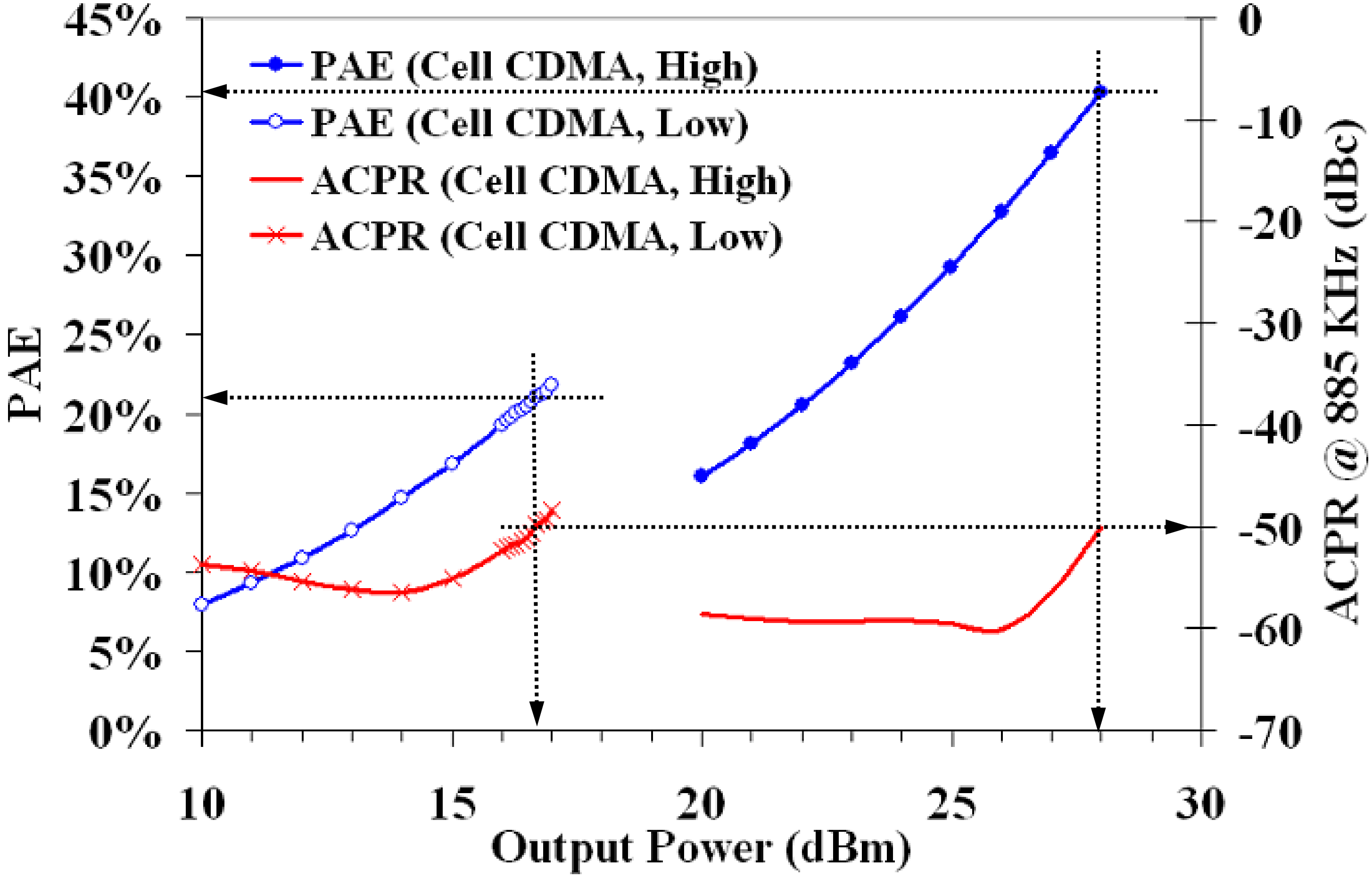


Split Line Spiral Single Layer

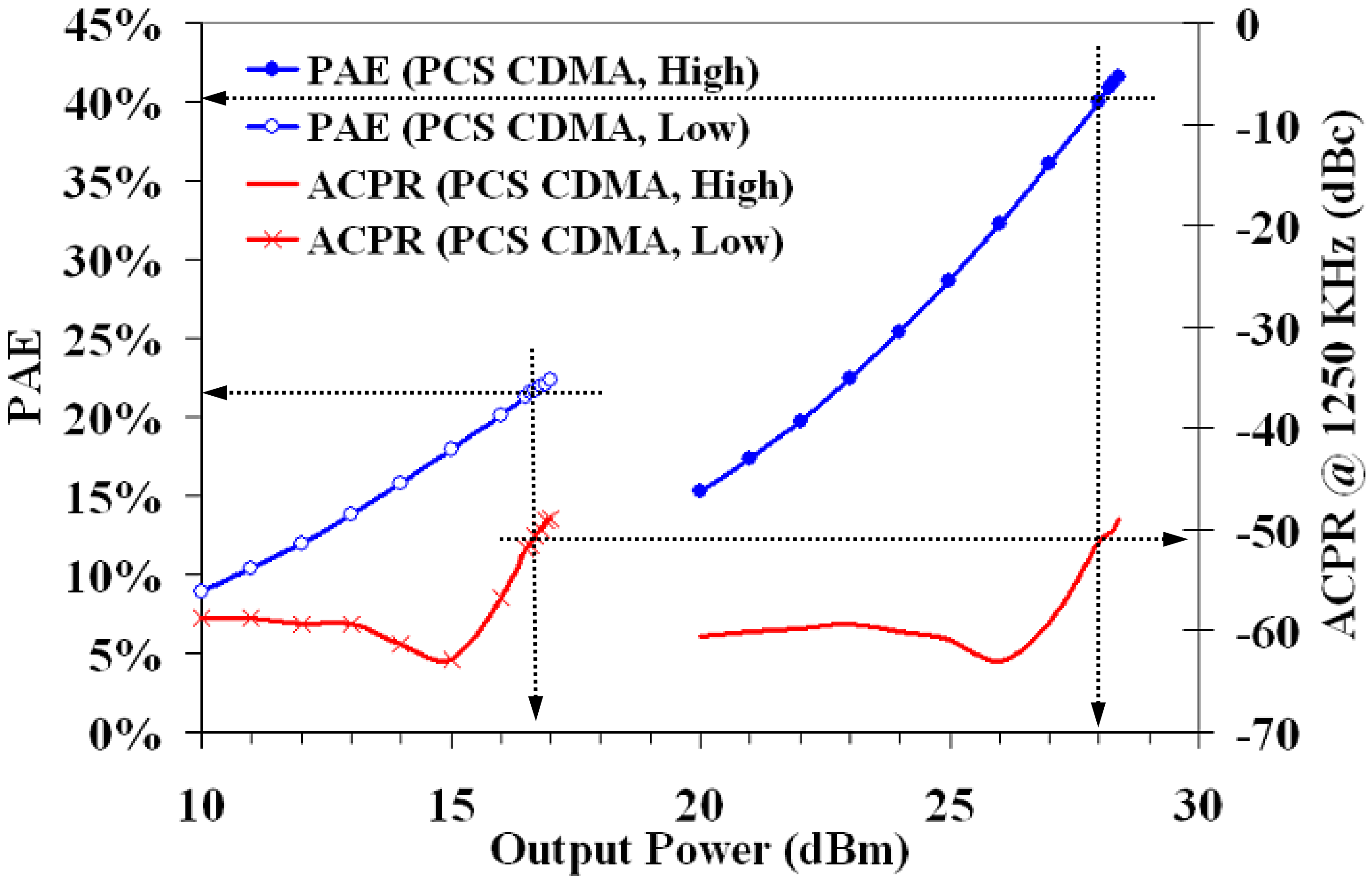


Broadside Coupled Split Line Spiral

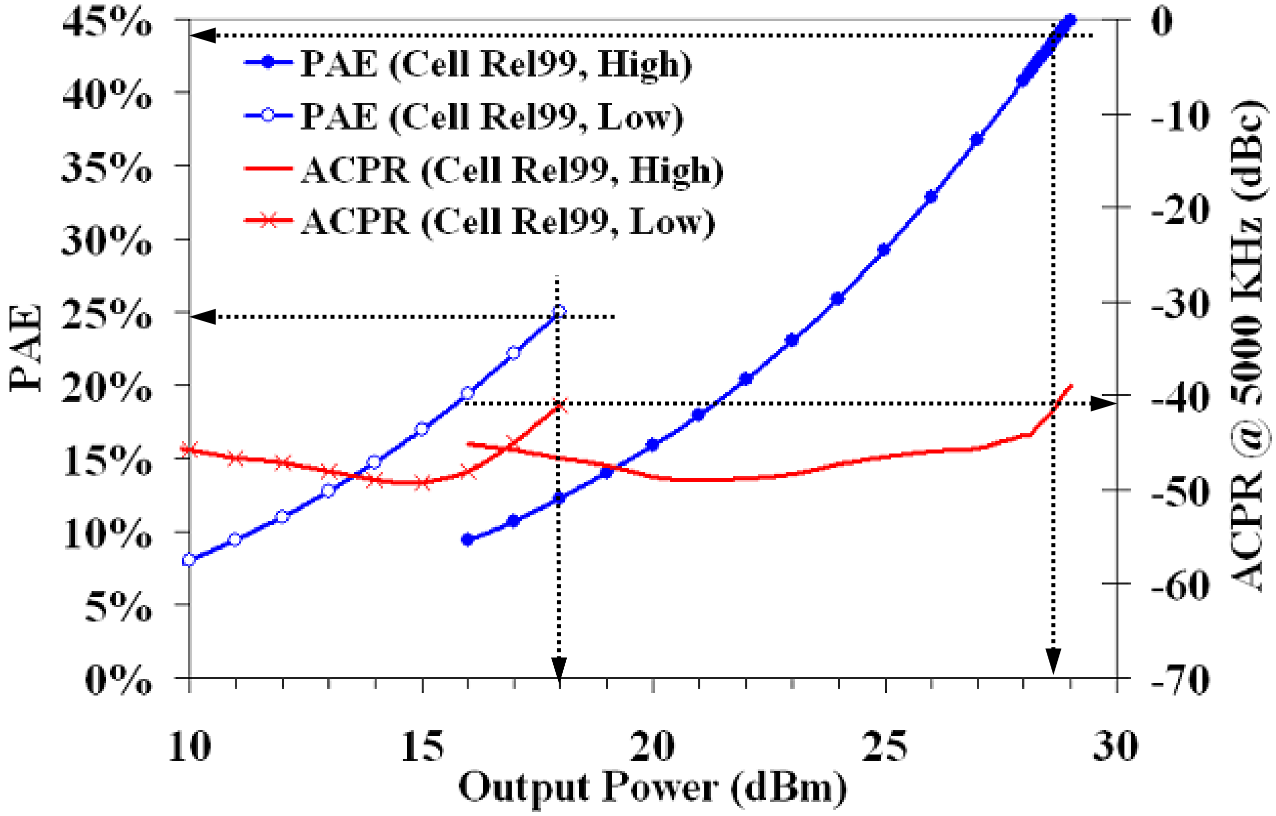
Cellular CDMA Performance



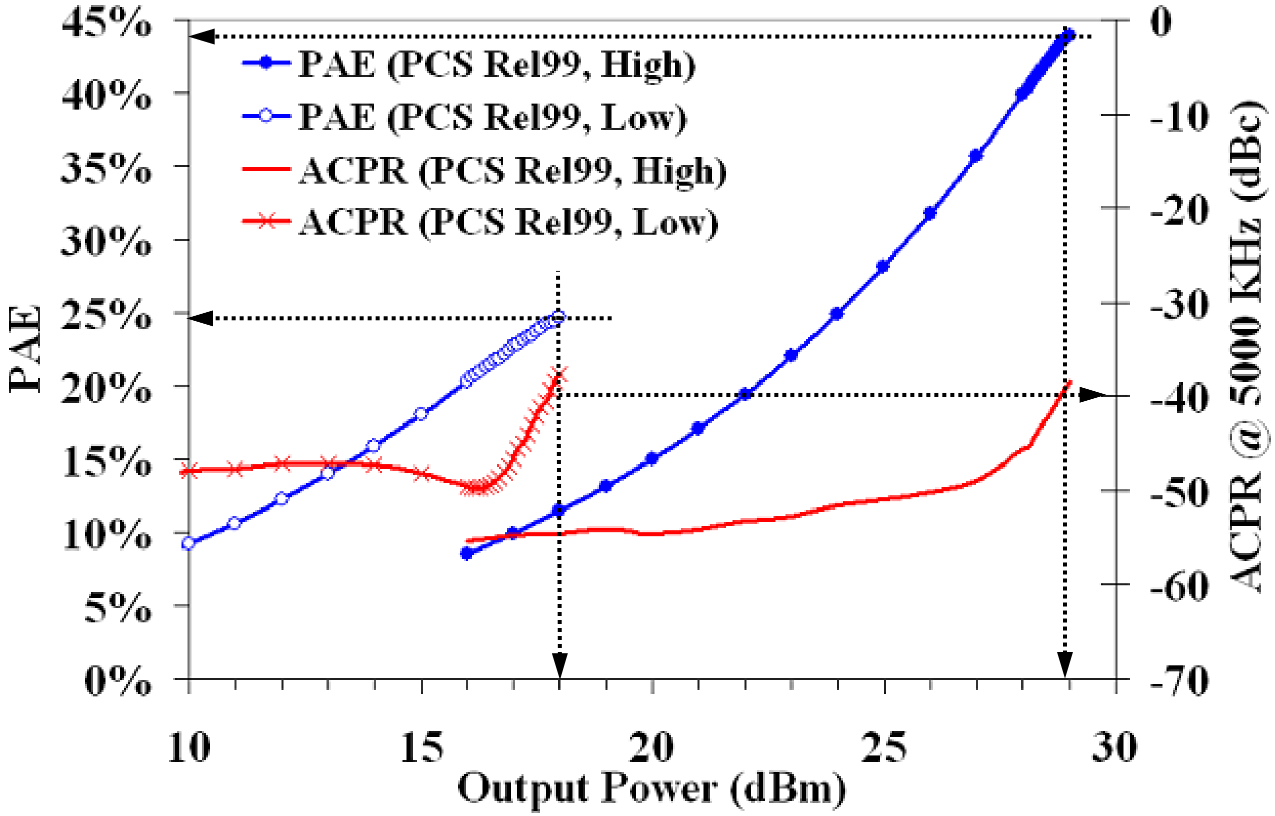
PCS CDMA Performance



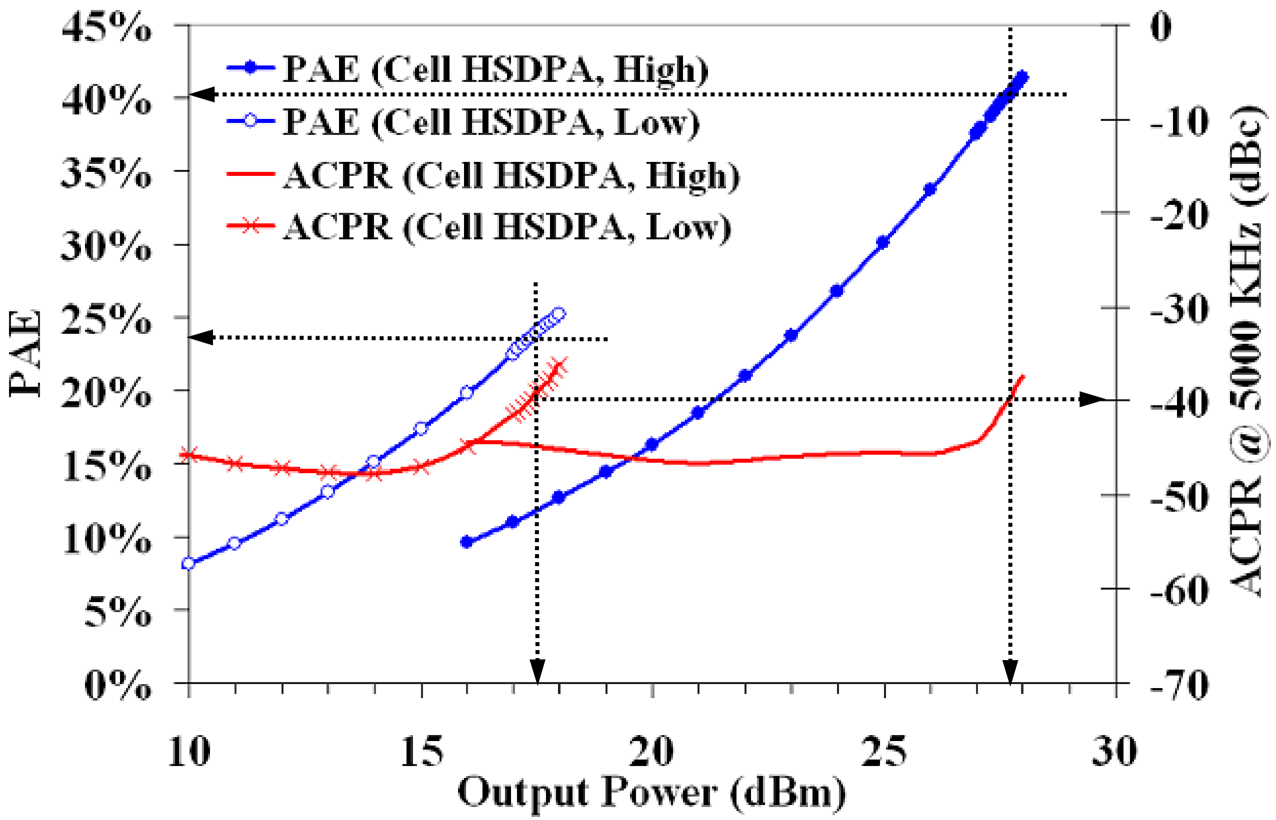
UMTS Cellular WCDMA (Rel.99)



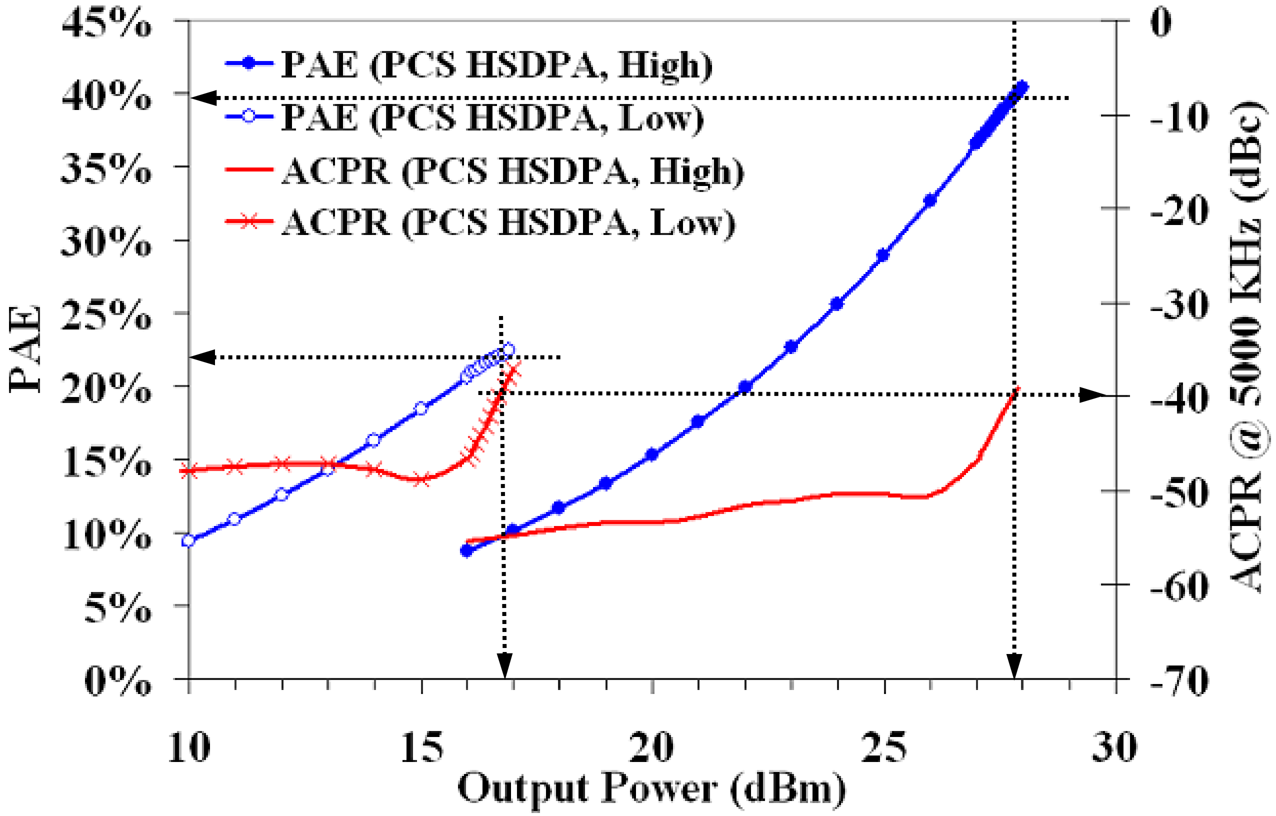
UMTS PCS WCDMA (Rel.99)



UMTS Cellular WCDMA (HSDPA)



UMTS PCS WCDMA (HSDPA)



Improvement: Tristate Switched Doherty

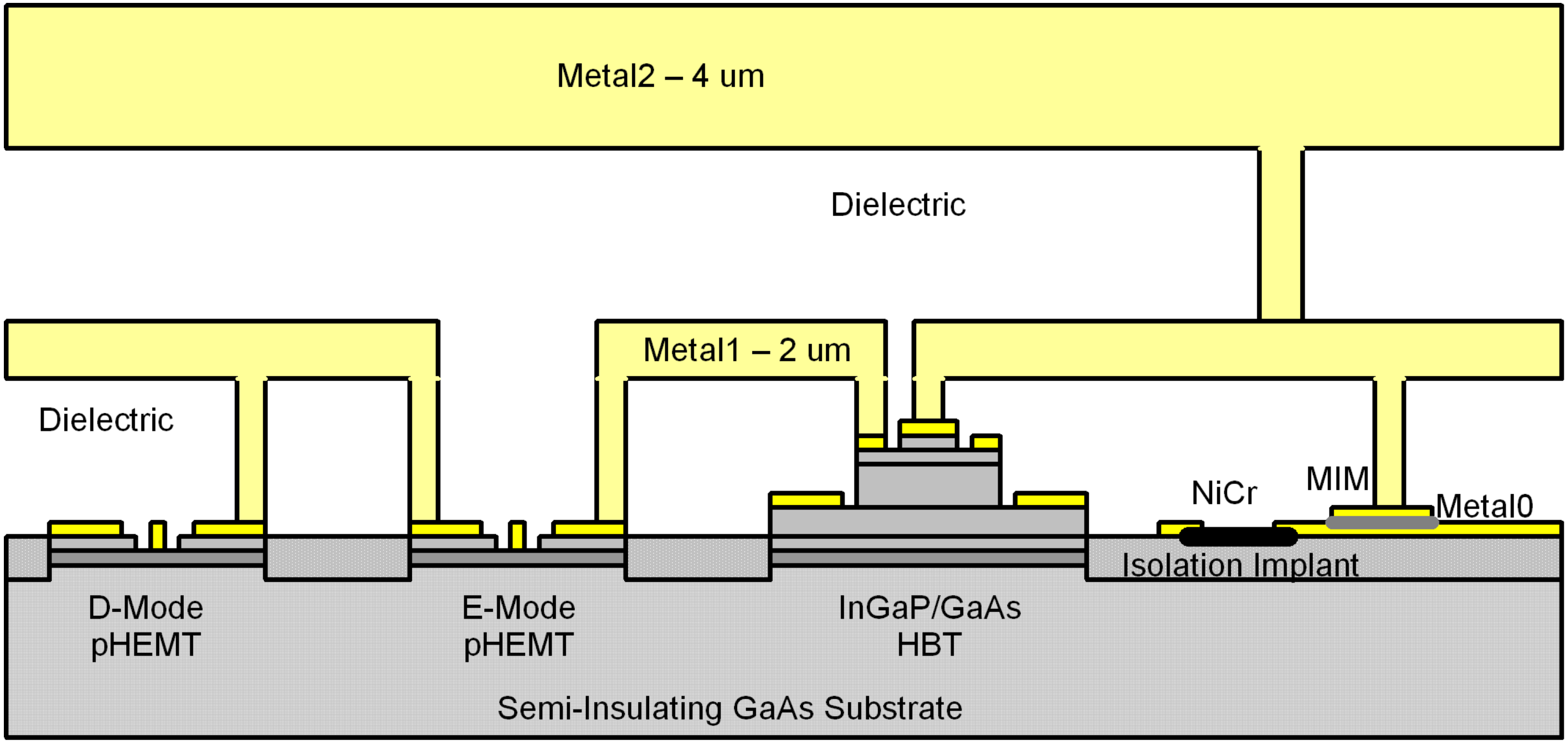
- Tristate (2-bit) power control.
- Build on switched Doherty (2-state) core
- No Vref needed -- PA operates directly from Vbatt.
- Enabled with logic interface (< 100uA control)
- Back compatible into standard sockets Vref pin is replaced by "*ENABLE*" logic input.
- Quiescent currents:
  - 6 mA **!** ultra low power mode,
  - 25 mA low power mode, and
  - 78 mA high power mode.

Approach

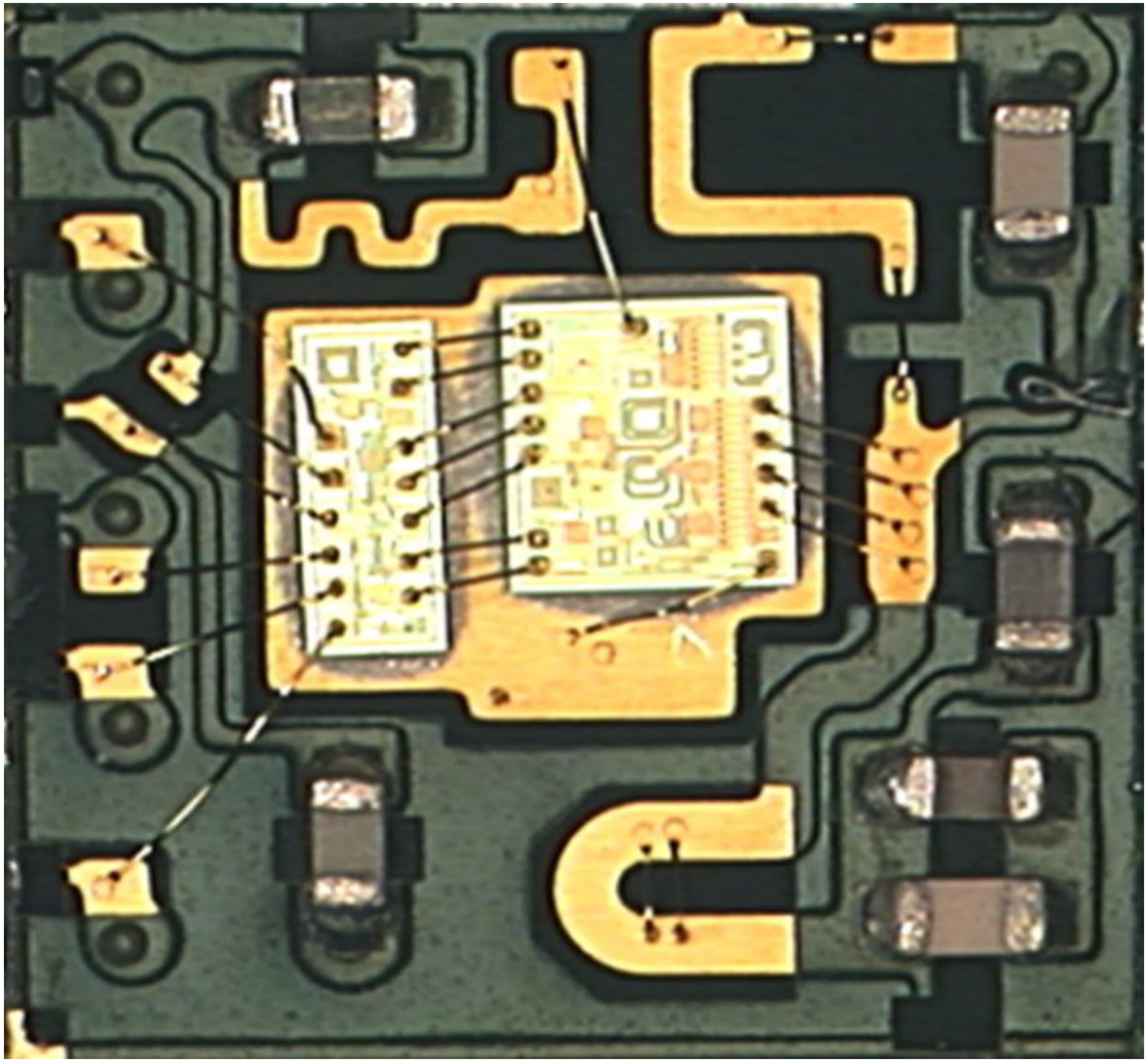
BiHEMT process enables integrated solution:

- Switched Doherty PA core in HBT
- VREF elimination with pHEMT current sources for HBT bias circuits
- Low current logic pHEMT
- RF switch in pHEMT

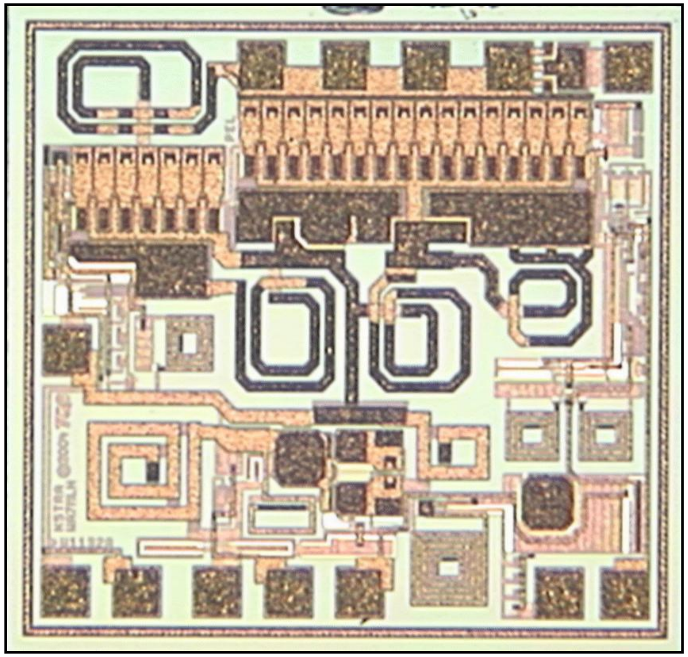
BiHEMT: Co-integration of HBT and pHEMT



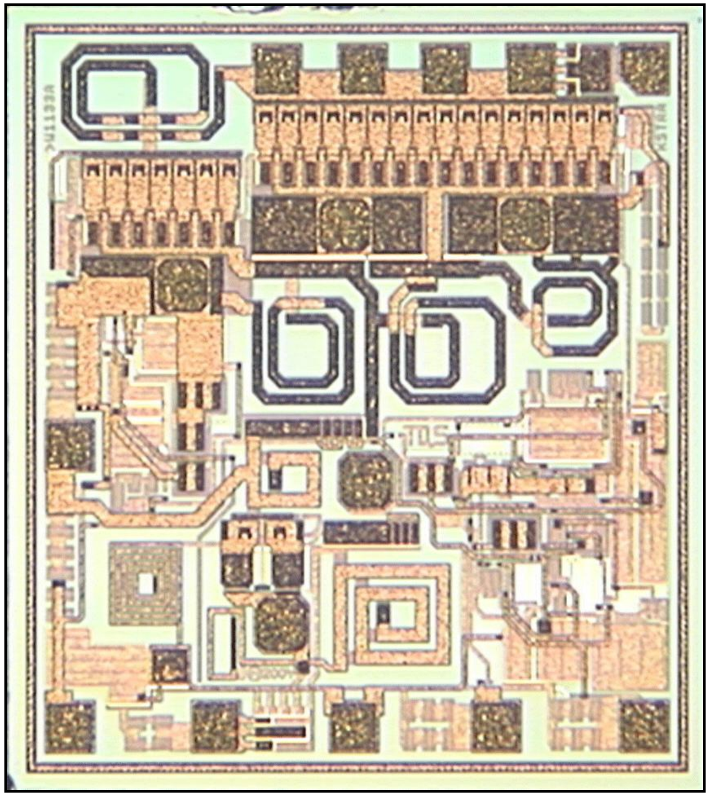
Tristate PA Module with pHEMT and HBT Chips



HBT PA Size Reduced from Original Switched Doherty



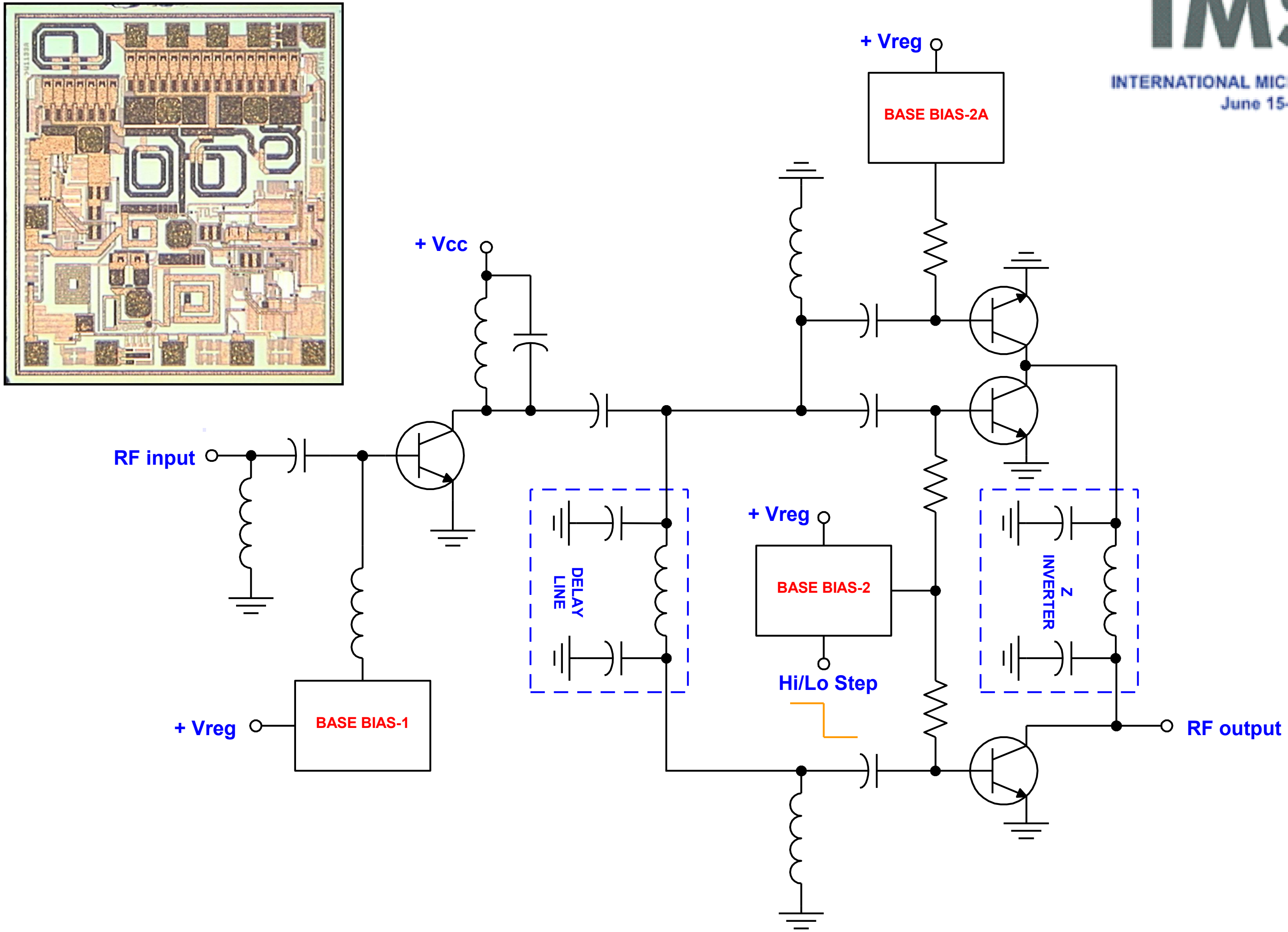
TRISTATE HBT PA



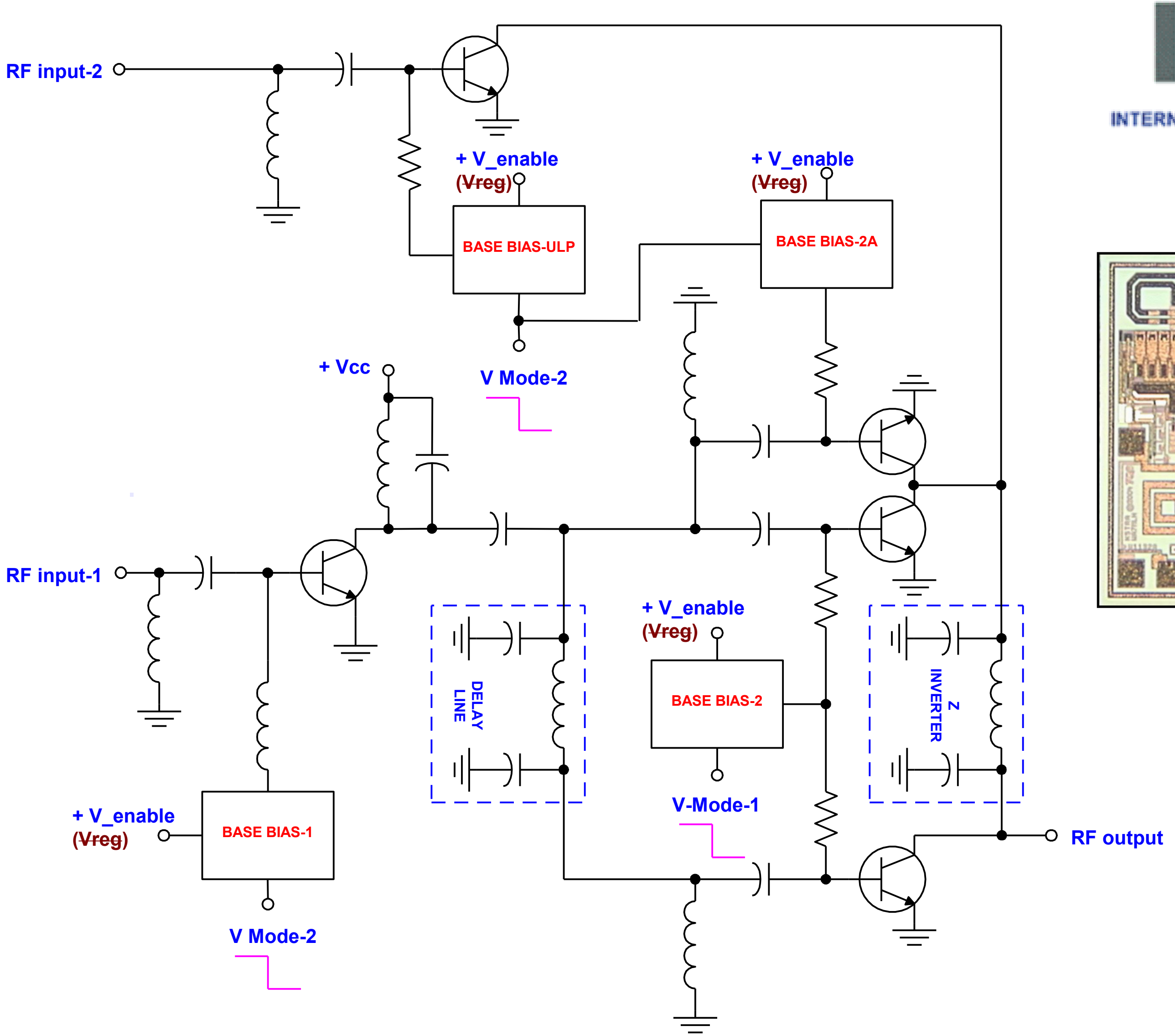
ORIGINAL SWITCHED DOHERTY

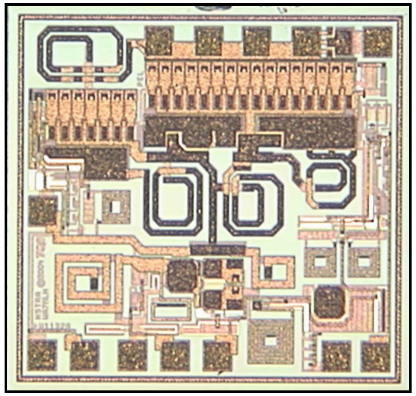
- Builds on original architecture
- HBT PA area is substantially reduced due to removal of complex bias and control circuitry
- Type-1 or type-6 current mirrors are designed to be driven by the Bias-Control chip

Switched Doherty PA Core (2 state)

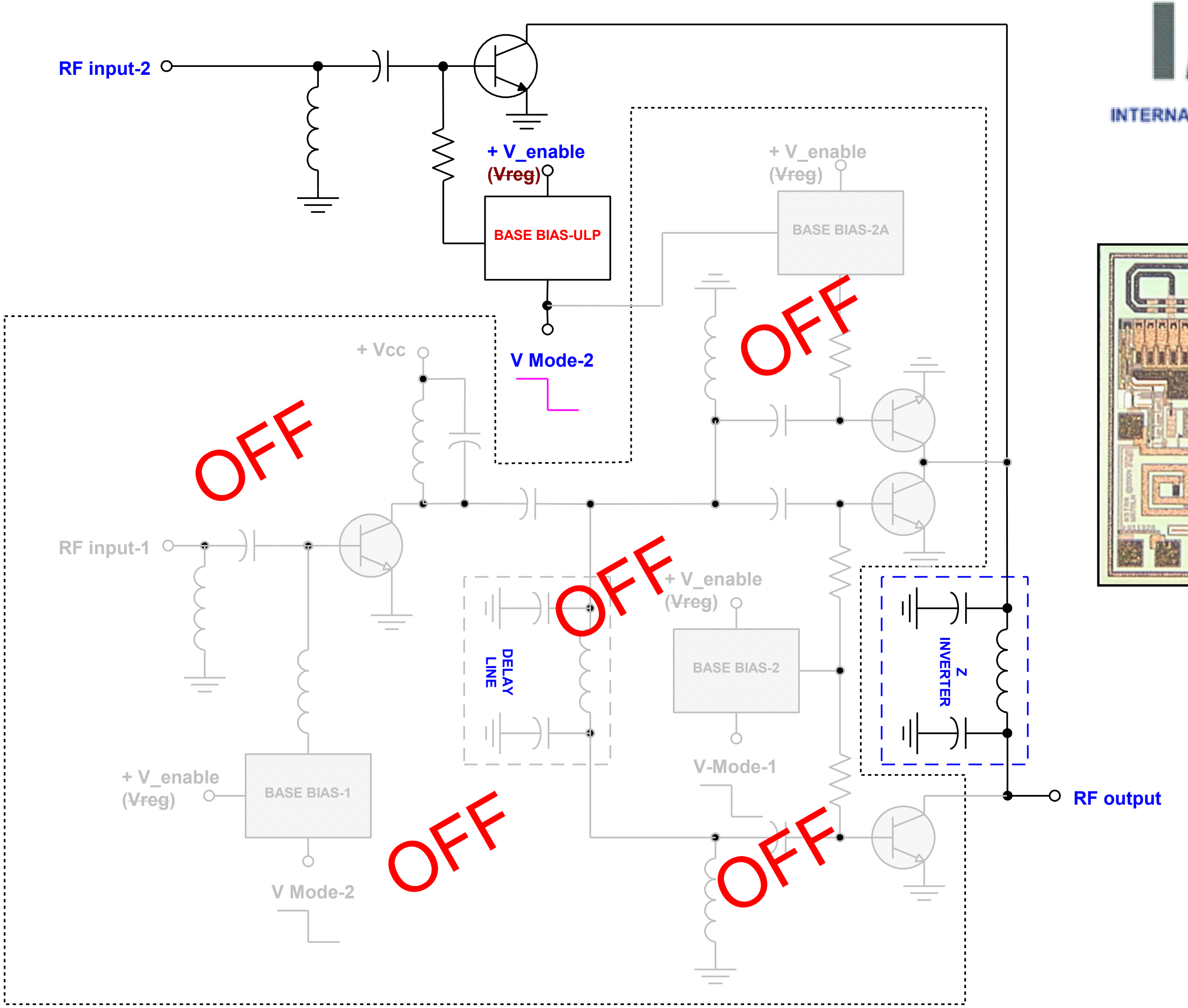


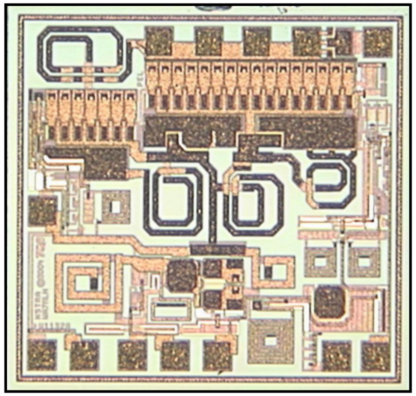
Tristate Switched Doherty PA



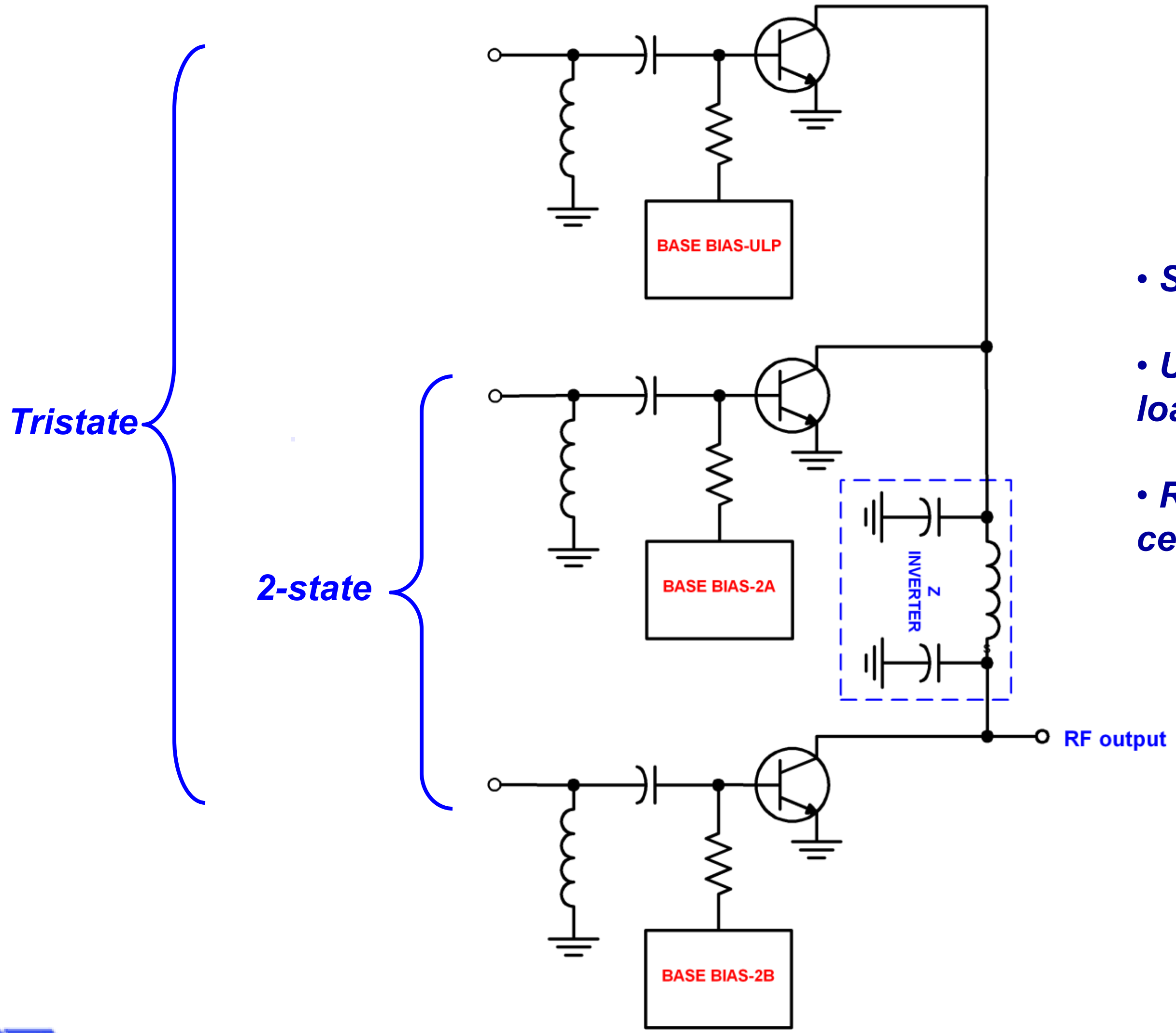


Ultra-Low Power Mode





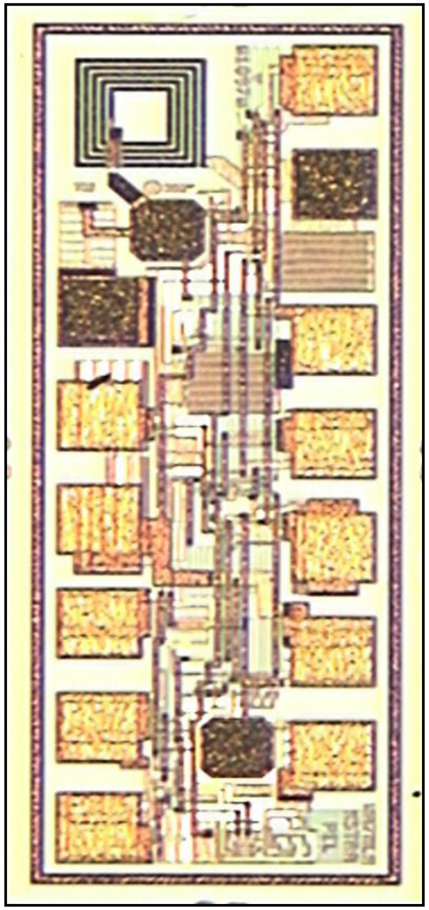
Simplified View of RF Loading in Tristate PA



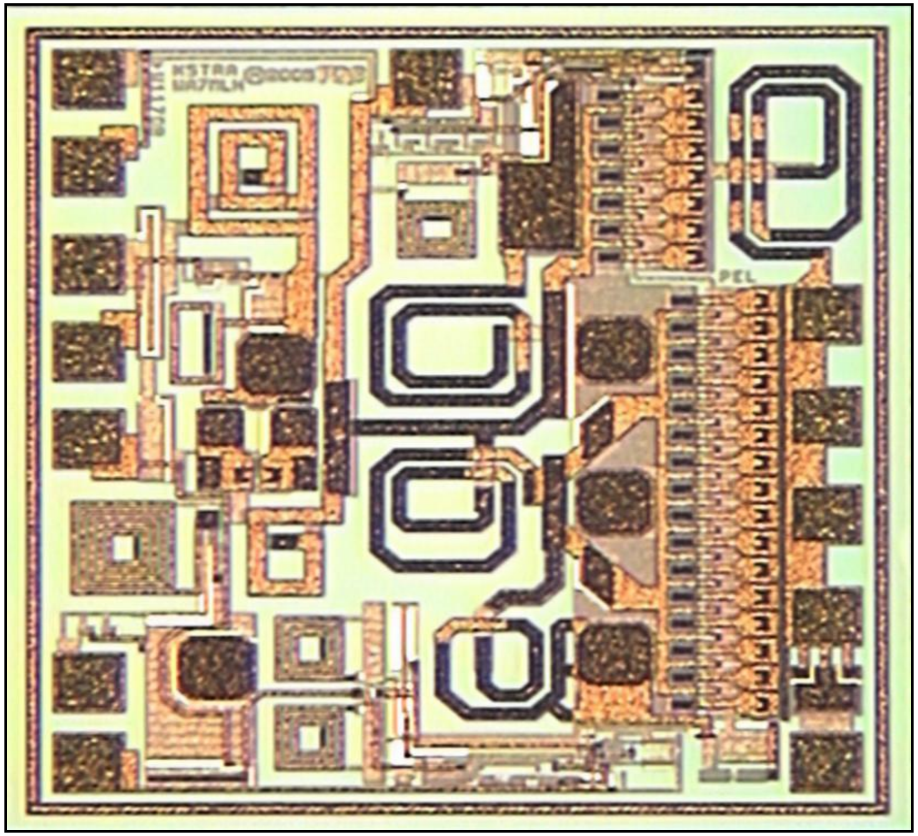
- *Switched Doherty 2-state core*
- *Ultra-low power mode uses load from low power mode*
- *RF input switch drives single cell in ultra-low mode*

Separate pHEMT and HBT Chips

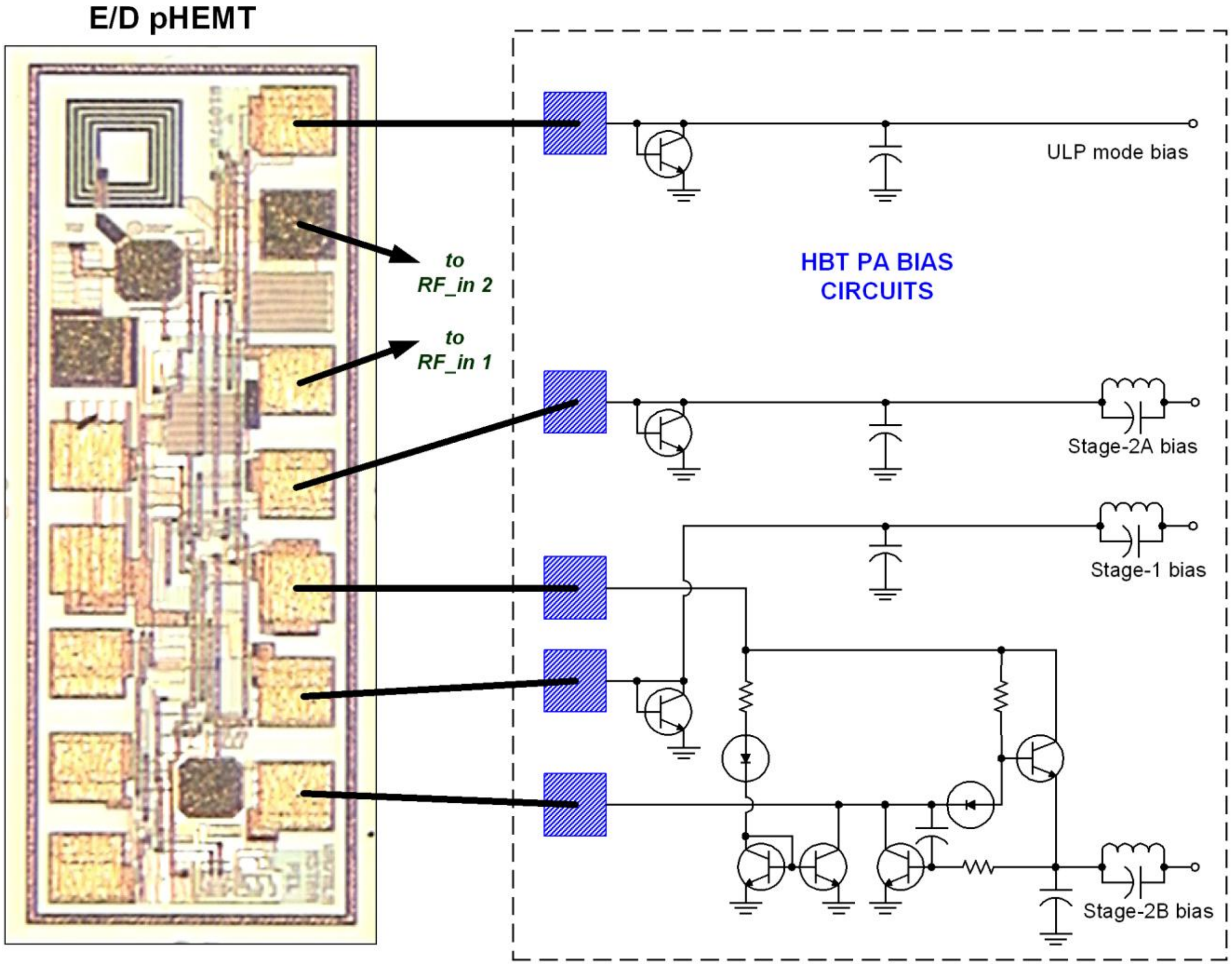
pHEMT BIAS / CONTROL



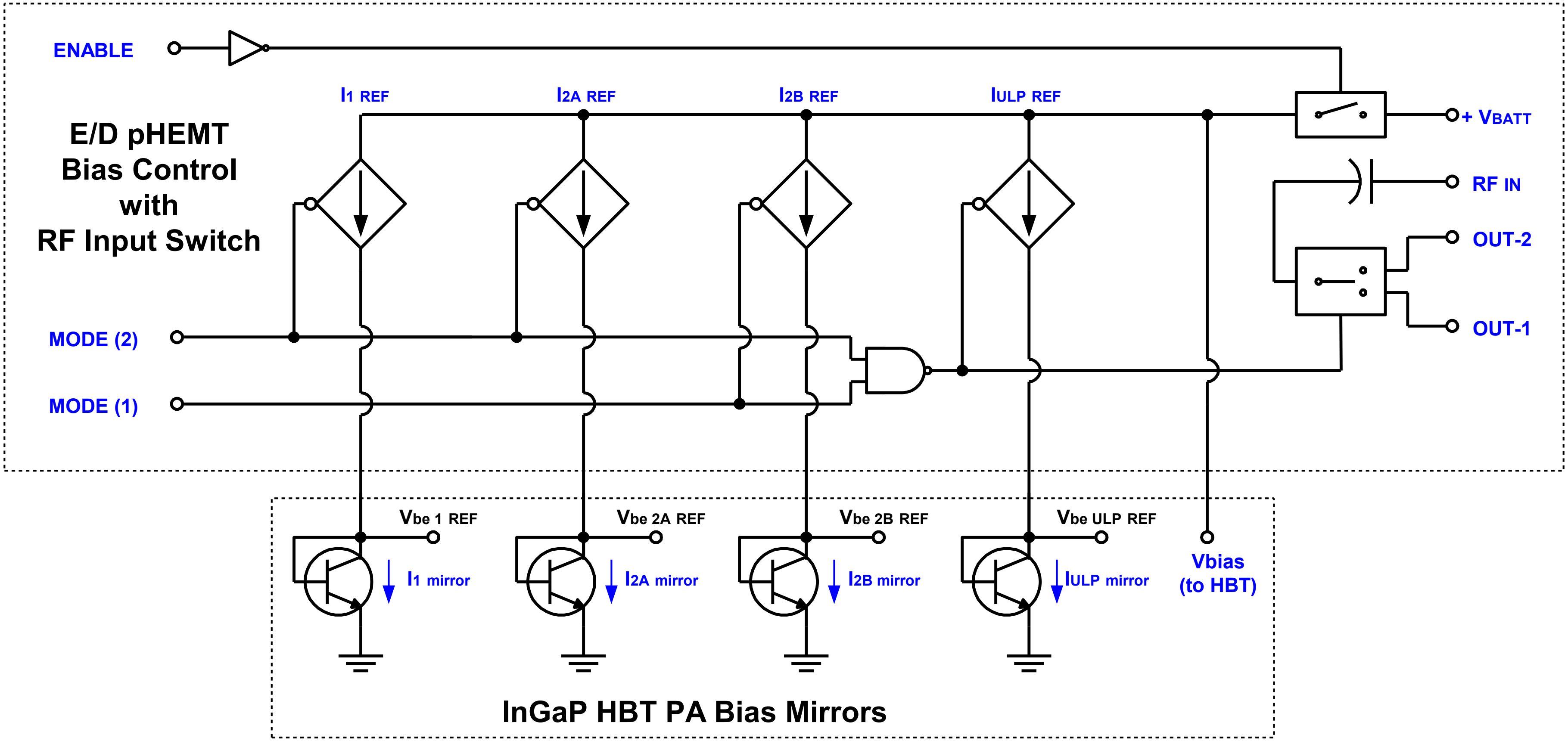
HBT POWER AMPLIFIER



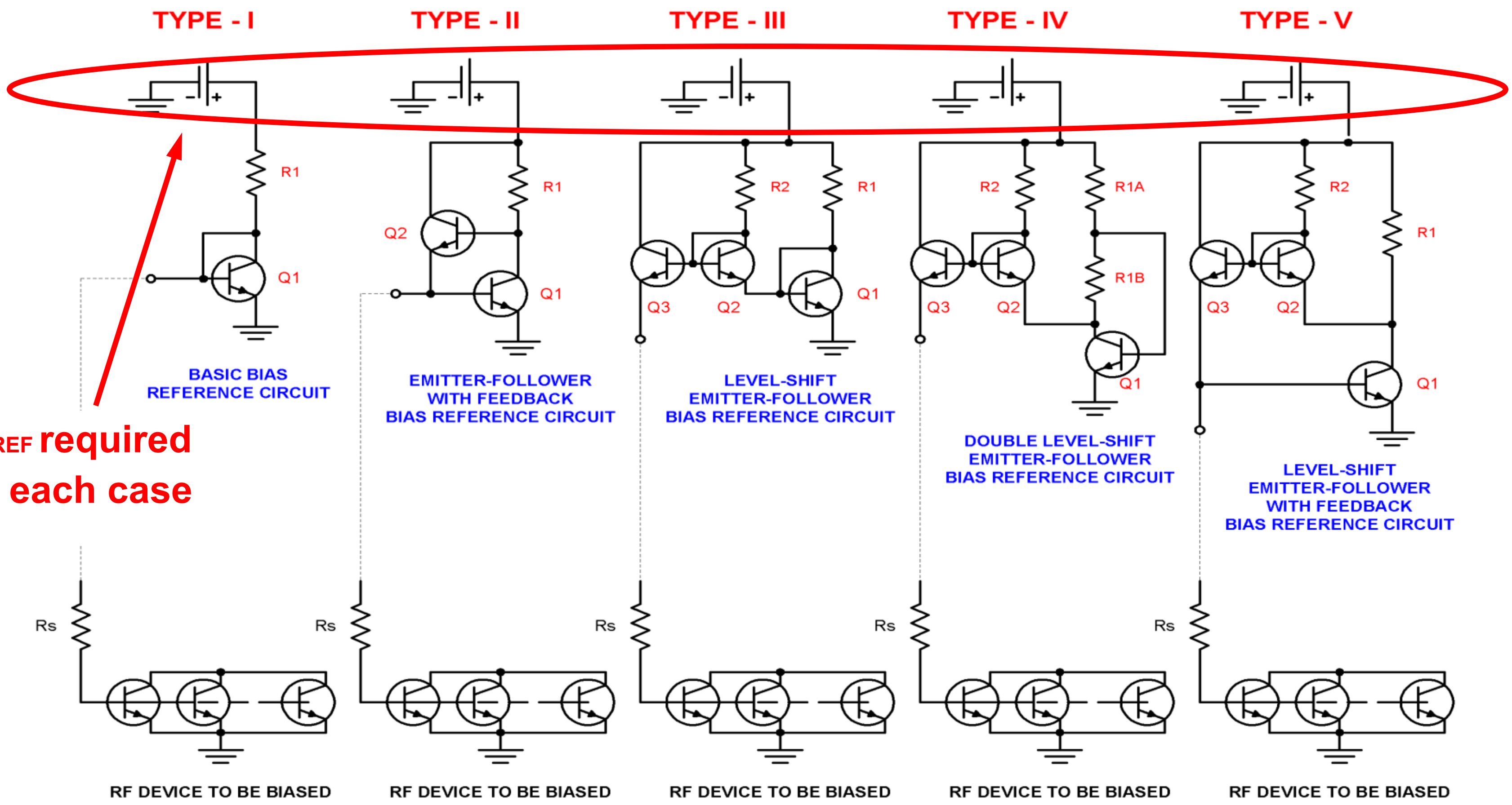
Bias Control ⇨ PA Interface



E/D pHEMT Bias Control with HBT PA

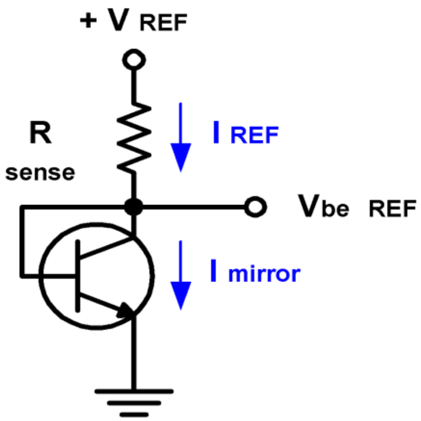


Standard HBT Bias Reference Circuits



V_{REF} required in each case

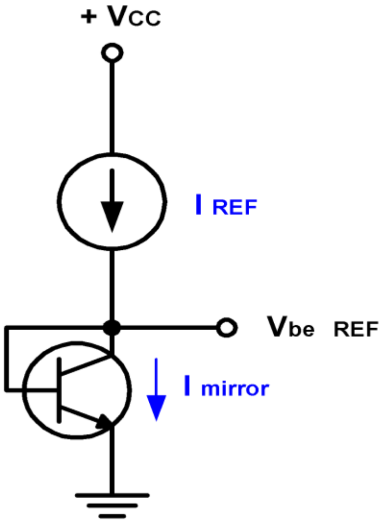
Elimination of VREF



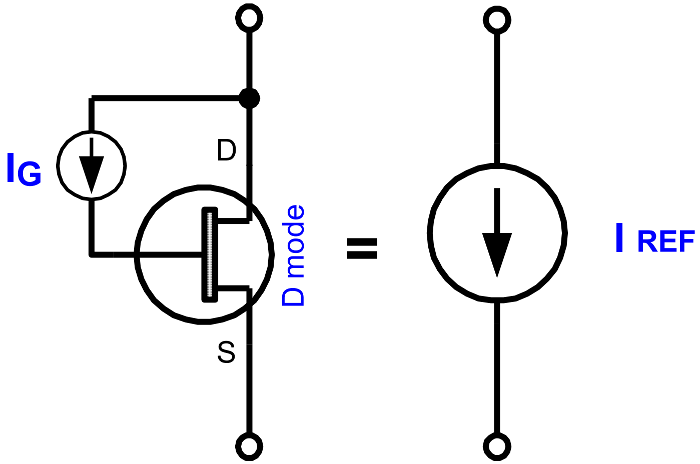
- Current density is mirrored in RF (biased) device
- I_{REF} set by $(V_{REF} - V_{be})/R_{SENSE}$
- Precise control of V_{REF} required
- Low Z_{SOURCE} requires high I_{MIRROR} (and high I_{REF})

TYPE-I BIAS MIRROR REFERENCE CIRCUITS

- Current density is mirrored in RF (biased) device
- I_{REF} set independent of V_{REF} by current source
- Low Z_{SOURCE} is easily obtained since current flows from Vcc (V_{BAT})

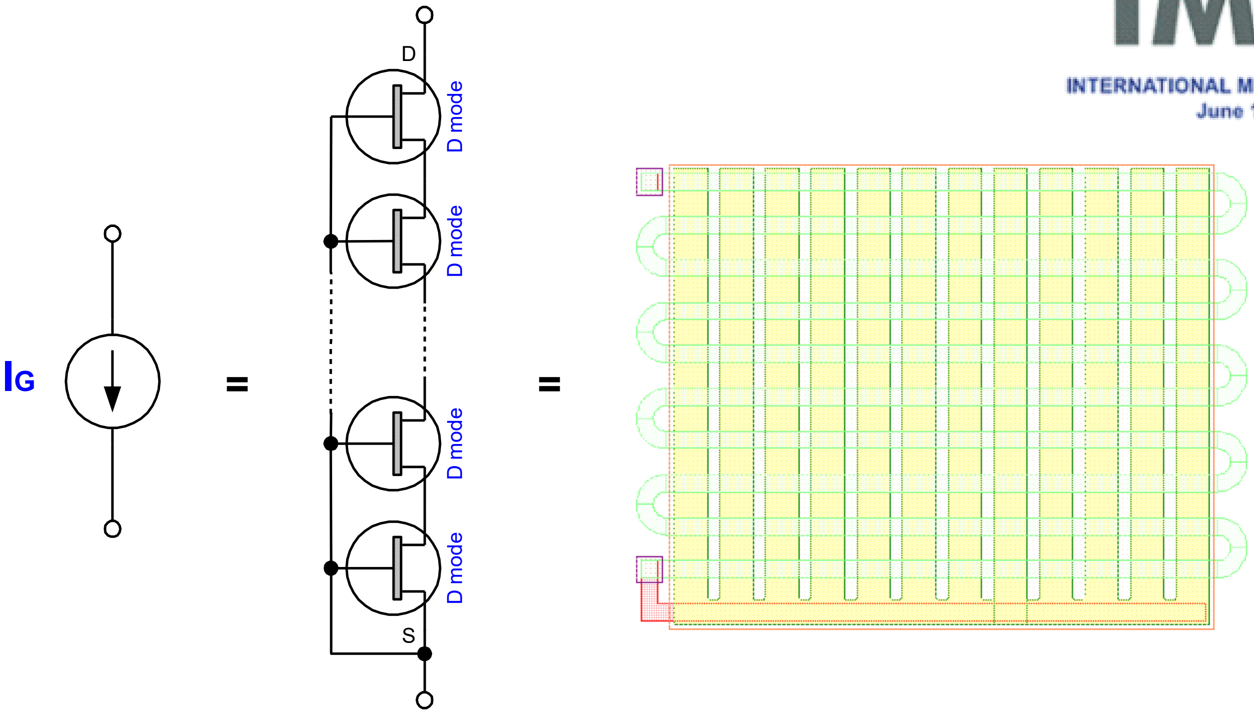


Current Sources for Bias Circuits



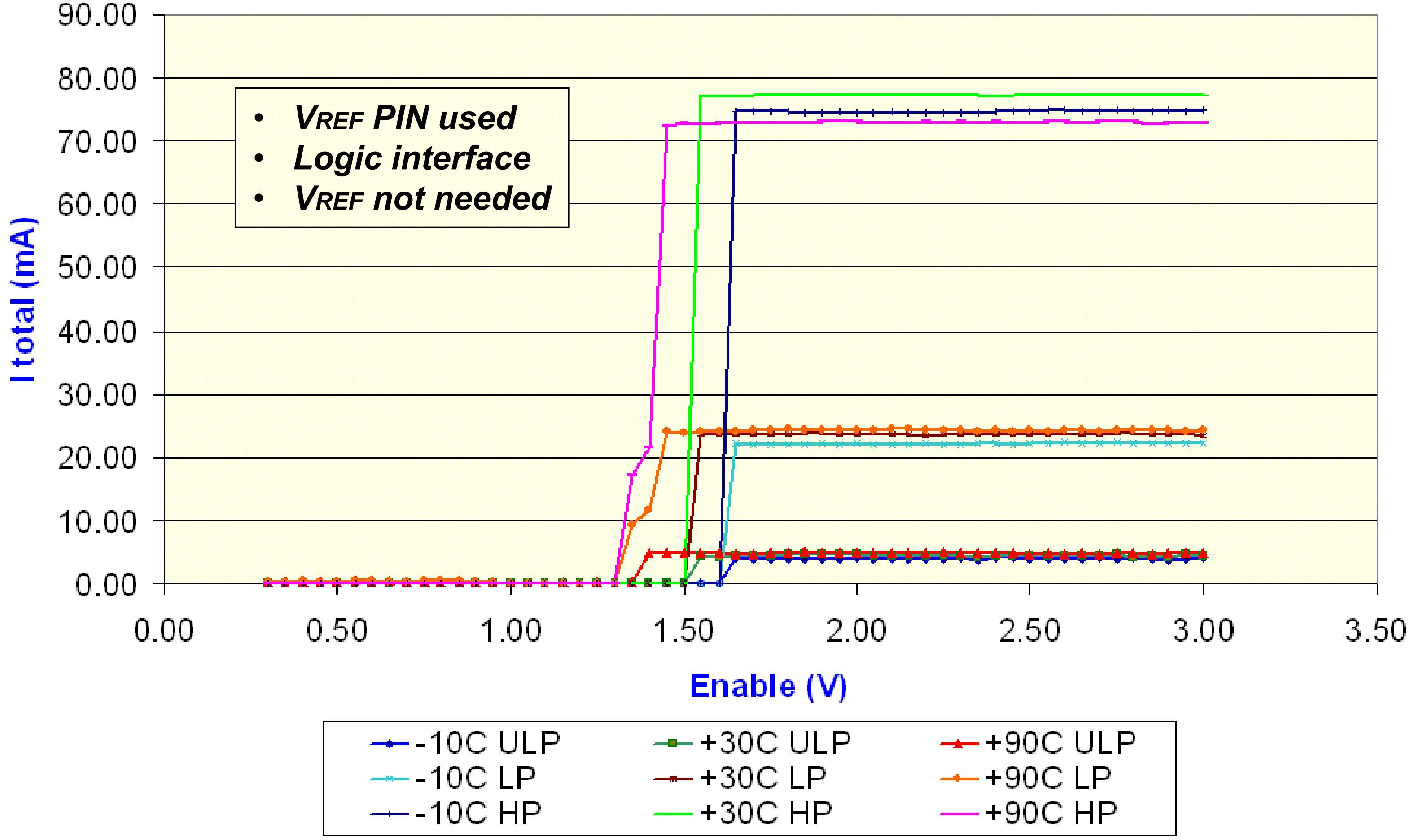
- **pHEMT I_{MAX} is well behaved (epi dependent)**
- **$\sigma < 7\%$ ($3\sigma = 20\%$)**
- **Geometry scaled to set current**

I_G Pull-up for Imax Operation of Reference FET



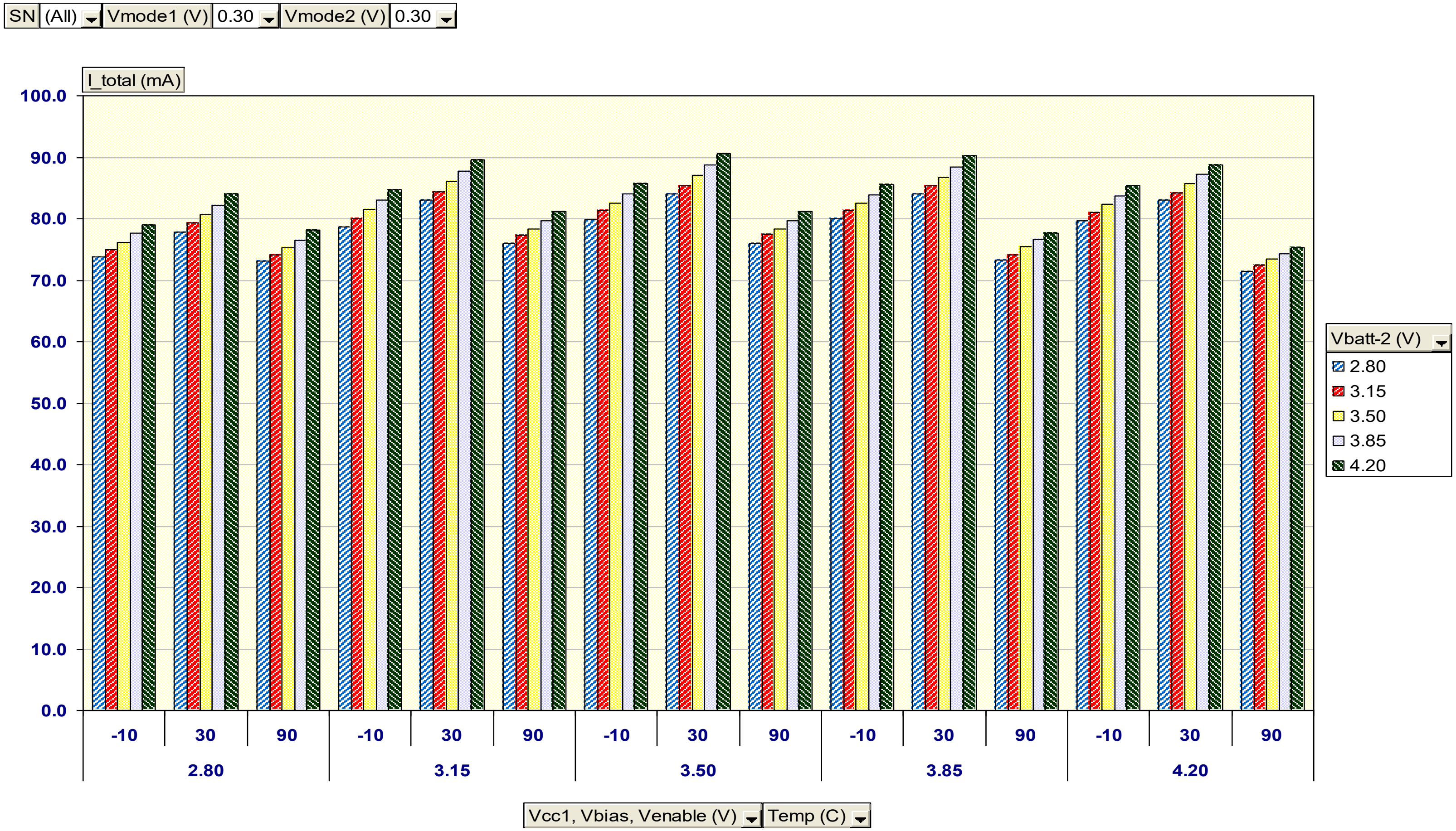
- I_G < 1 µA
- I_G is dependent on I_{dss} (a wide distribution)
- s = 16% (3s = 48%)
- Tight control of I_G is not important

PA Enable

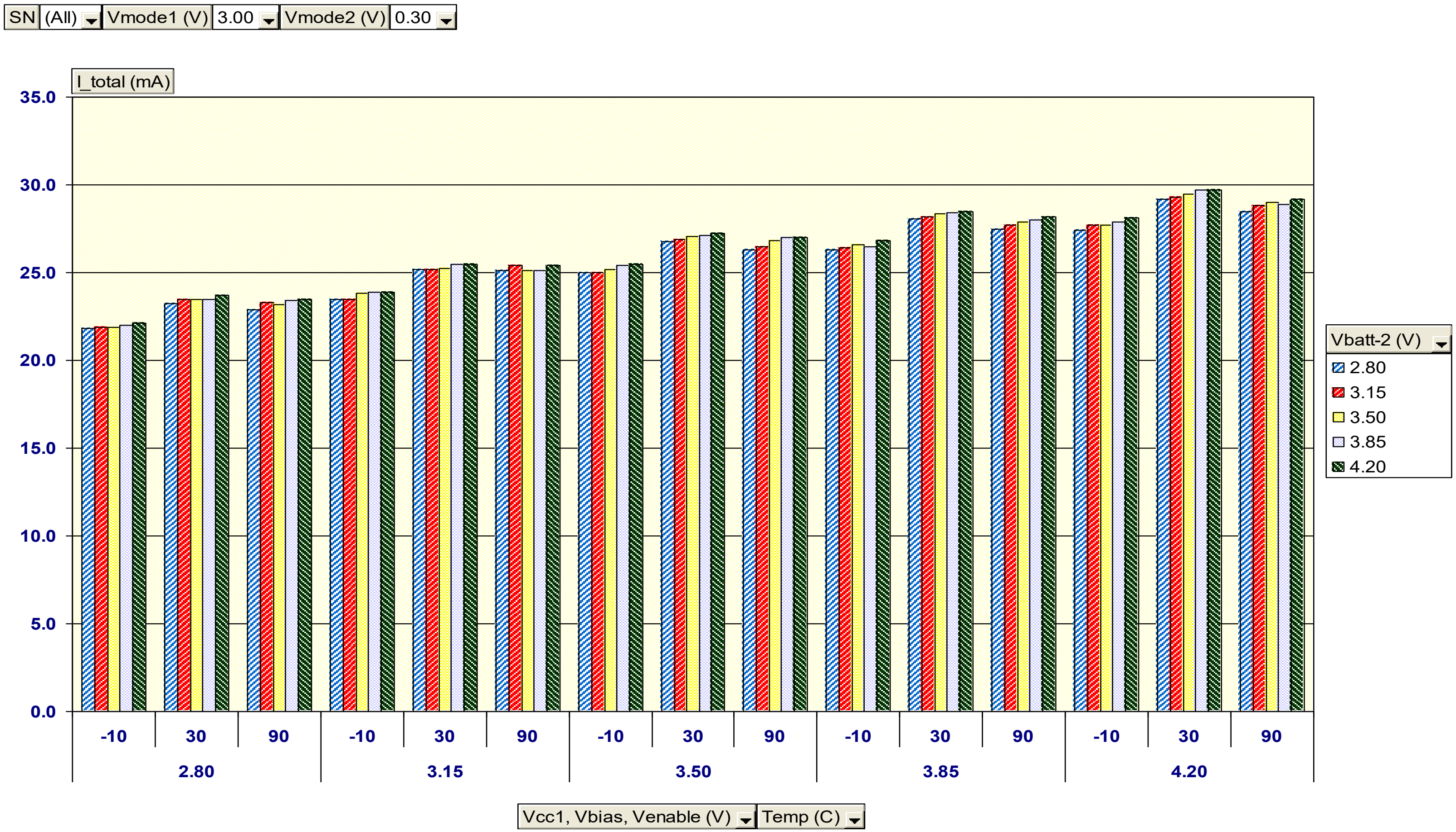


- *VREF PIN used*
- *Logic interface*
- *VREF not needed*

High Mode Quiescent Current

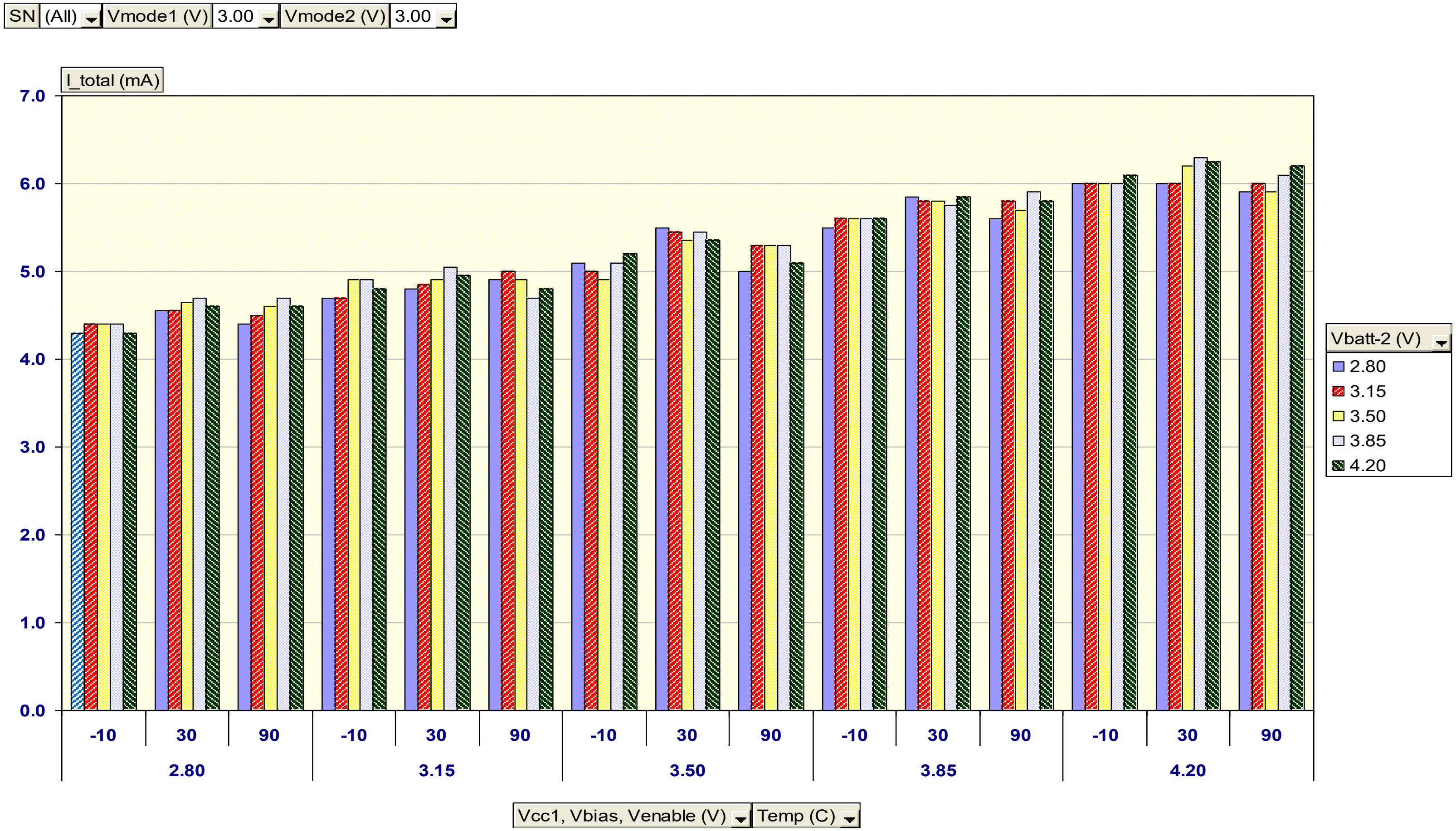


Low Mode Quiescent Current

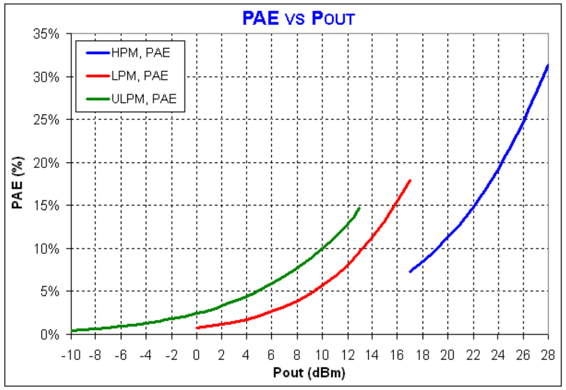


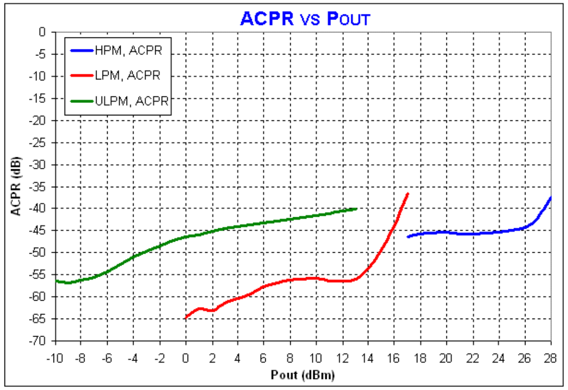
SN (All) Vmode1 (V) 3.00 Vmode2 (V) 0.30

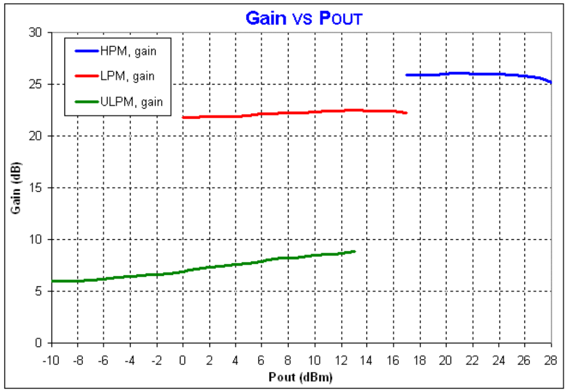
Ultra-Low Mode Quiescent Current



Tristate Switched Doherty PA Data


PAE vs Pout

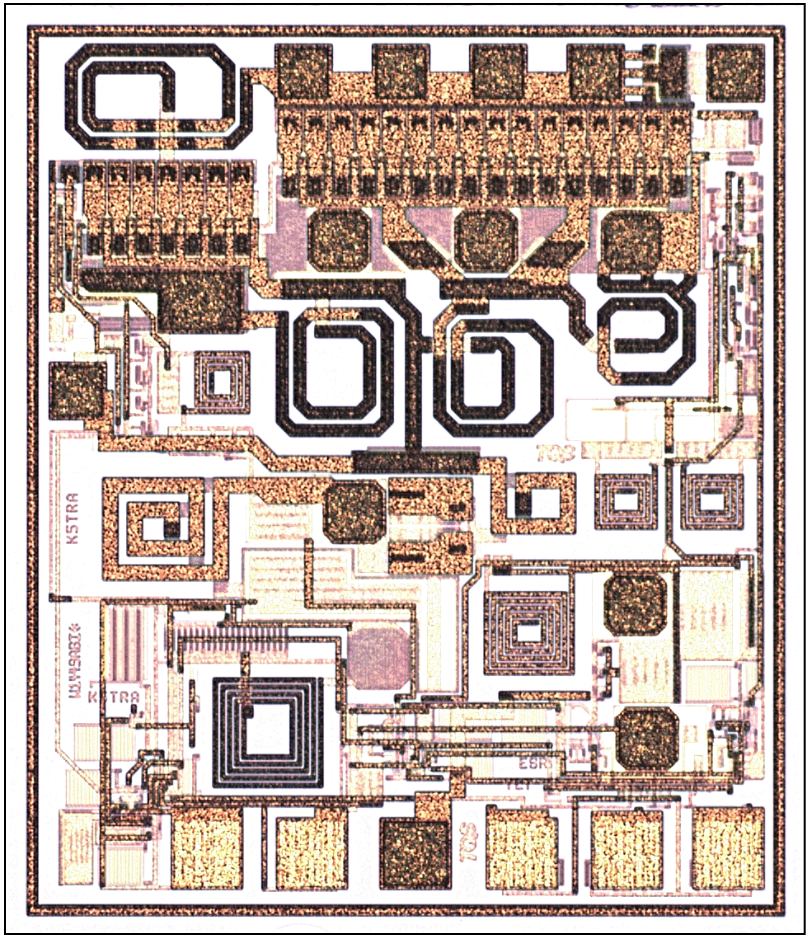

ACPR vs Pout


Gain vs Pout

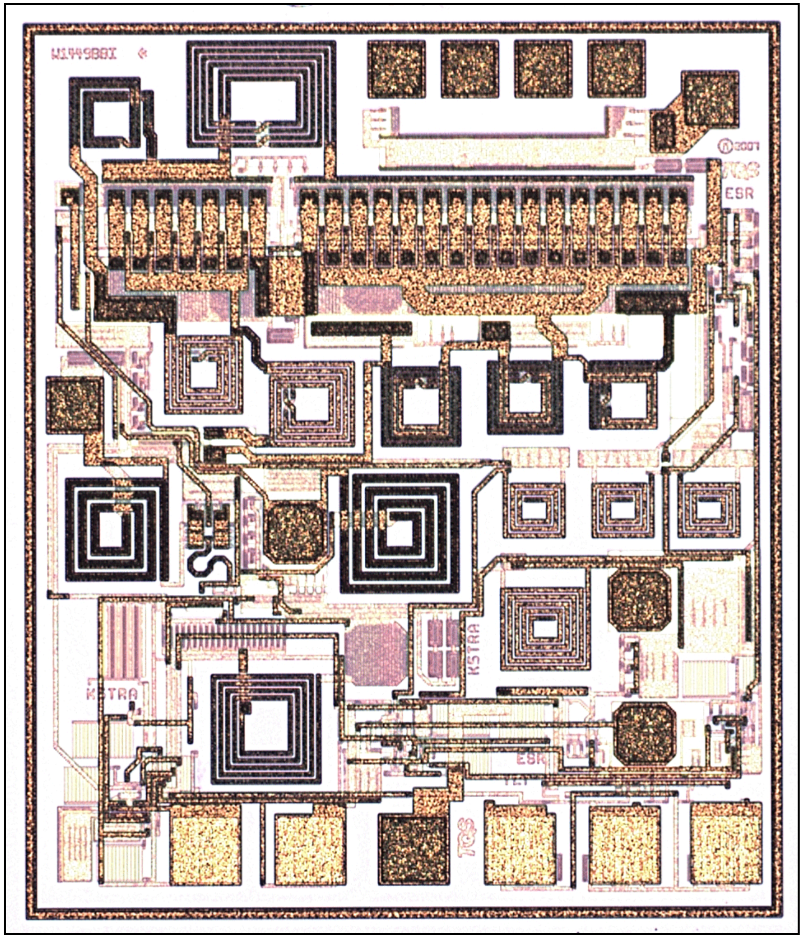
- Switched Doherty performance extended to ultra-low power mode
- Quiescent current typically below 6 mA in ultra-low mode
- Ultra-low mode supports up to +12 dBm with -40 dBc ACPR

BiHEMT Tristate Switched Doherty

1st GENERATION SWITCHED DOHERTY CORE



2nd GENERATION SWITCHED DOHERTY CORE



Conclusion

- Switched Doherty PAs have been realized in both PCS and Cellular bands for linear operation.
- Power efficiency and linearity are quite good in both high and low power operation.
- Basic switched Doherty architecture has been extended to Tristate operation with extremely low quiescent current in the lowest power mode
- BiHEMT process enables integration of pHEMT and HBT circuitry in Tristate PA
- Several techniques to improve performance have also been presented:
  - A new HBT geometry provides reduced C_{BC}
  - Use of low Zo interconnect structures to reduce inductance in base feed manifold
  - Use of composite split-line and overlay (broadside coupled) inductors for better area efficiency and good Q
- CDMA talk-time is significantly increased.

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